Silicon Integrated Systems Corp.

SS72 for SiS-55X Single Chipset
Uniprocessor Reference Design Schematics
Revision 0.9 (July 8, 2002)

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LINK
SS72A-2.SCH
SS72A-3.SCH
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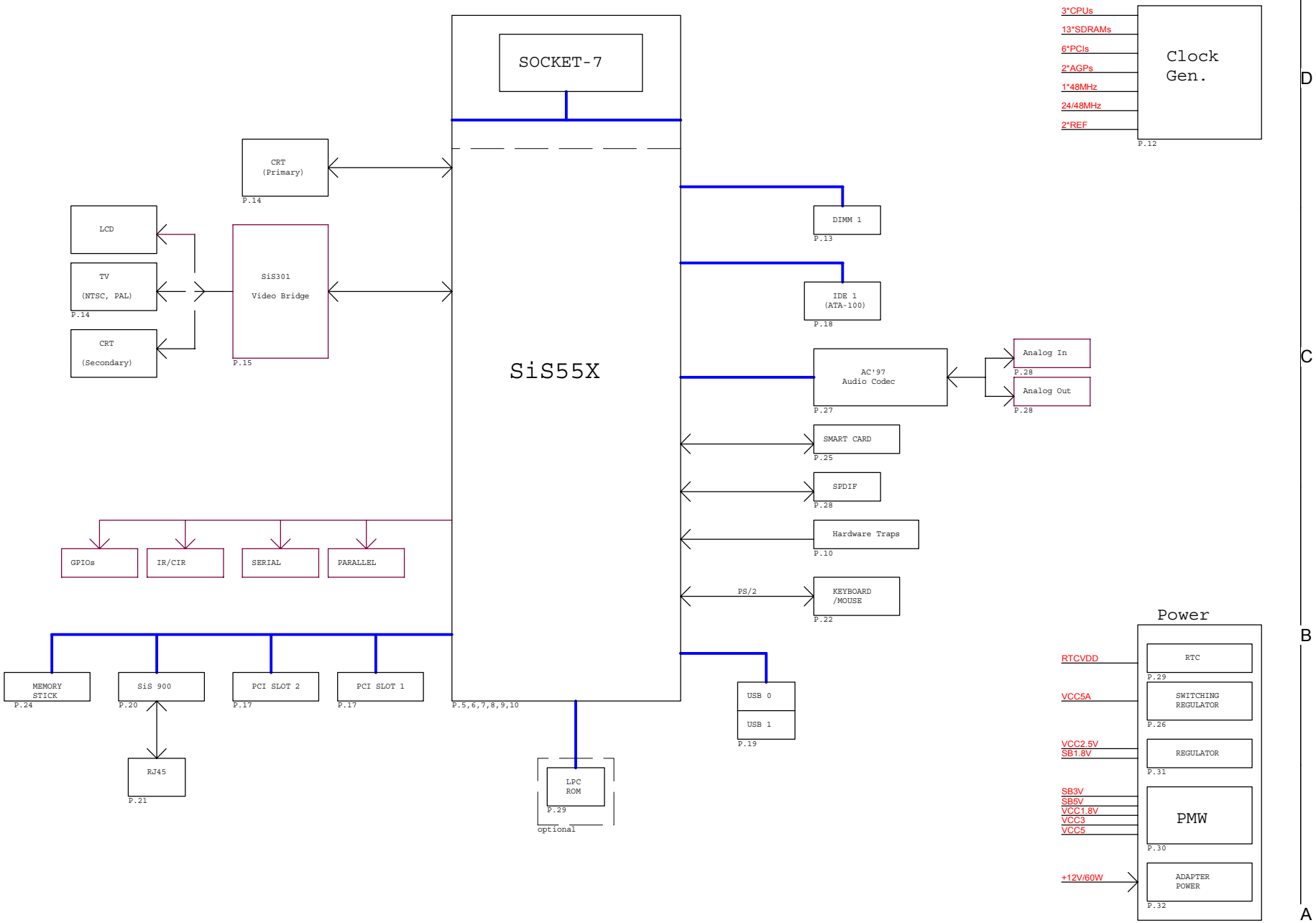
System Block Diagram



SILICON INTEGRATED SYSTEM CORP.		
Title: 550 System Block Diagram		
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DATE	Rev	Description	Page
2000/9/6	0.1	1. Initial release	
2001/3/16	0.8	POWER SYSTEM CHANGE CAN SAVE MORE THAN 50% COST WE USE MOSFET TO SWITCH SB5V,SB3V INTO VCC5,VCC3 INSTEAD OF REGULATOR AND VCC1.8V FOR CORE POWER USE LOW-END SWITCH REGULATOR INSTEAD OF PWM USED FOR CPU	30,31,32
		ROM1 for Smart Car should fed SB5V not VCC5	25
		We add two LEDs,Red for SB5V,while VCC5 on,Red LED turn off and Red LED on.	26
		U31(LT1613)PIN4 should contact with VCC3 to enable itself.	27
		Add feature connector	16
		Add SLOT HOLE FOR SiS550 IN PCB	
		BOTTOM DEFIND WRONG(B1,B2,B3)	
		ADD NC PAD BETWEEN PSON# ADN GND	31
2001/4/10		PUT CKE[0..1] HIGH WITH 4.7K	12
		Add R1FCLKDVI4 TEST PAD	5
		RAD4,RAD6 PUT HIGH , RAD[0,1,2,3,5,7,8,9] PUT LOW	6
		Connect some NC pins of DSTN CONN. to the GND	13
		RGB Signals of DVI should add filter circuit	16
		Change HDDLED-0 jumper instead of LED.	26
		P1(LTP PORT),S1(S-VIDEO),J1(AUDIO JACK) Layout pin define error	23
		U14(IDEPWR CONN.) PIN DEFINE ERROR	18
		U18(IR) PIN DEFINE ERROR	23
		Remove SMART CARD LED	25
		Remove SMART CARD pin5 and pin9 juction	25
		FILT_R should add a same capacitor value with FILT_L	27
		Due to the RCA conn. color,we should tune the ap signals to meet its connector	28
		FLASH ROM power have VCC5 & VCC3 inputs with a jumper select	28
		Add some BULK capacitors to VCC5 and VCC3 in PCB	
		Change inductor value from FB to 2.7uH	14
		Add VCC3_DIMM for S3	33
		Change compoments value with AD1881 spec.	27,28
		Remove DDC2DATA & DDC2CLK from SiS55X to SiS301	7
		Cut VGA conn. ground into VGAD ground plane	13
		Add SO3 pad for RADD[0..3]	6
		Mux GPIO0 and PWRGD to B2(For GPIO Test and Reset function)	8
		Add Two Variable Resistors to tune DSTN Contrast and Brightness One Moudle for DSTN power	13
2001/6/13		Add 330uF on Q26 Drain and R214 path to GND to delay PWRGD signal for DOC and Q22,Q23,Q24 default value are NC	31
		D8(Red)for SB power and D9(Green) for Main power should connect to PS_ON not FN5235 powergood, cause FN5235 creat SB5V and SB3V,PWRGOOD already exit in AUX power	31,26
		Q14,Q16 for delay VIN to FAN5037 would demage by large current,due to RC5037 have no sofe star protect circuit to let gate drive turn on slowly We strongly recommand use FAN5037 instead of RC5037	32
		Change VCC5 to SB5V for Mouse power to fix setup time too short	22
		We recover RGB connector GND plane to default setting	13
		Modify Page 23 Label PRNINIT- to PRINIT- which connect to 55X together	23
		Remove C57,C59,C61,C64,C66,C90	16
2001/11/1		Swap RADD9<-->RADD10	6
		Change CE29,CE35,CE37 from 330uF to 470uF	32
		Change L36 from 8.2uH to 16uH/5A	32
		Change FDS4410 Gate Drive voltage from VCC5 to +12V	19
		Remove LDO3(78L05)	18
		Change J19 from short pad to open pad	18
		Change R242 to SO3_4.7K(J3) pad	6
		Add TFT LCD Panel control signals combine to JP4	13
2001/12/26		Modify PWRGD circuit	31
		Modify CIR circuit	23
		Change ROM power from VCC3 to SB5V for DOC	29
		Add DDC3DATA/DDC3CLK pull up resistors 4.7K to VCC3.	15
		Modify LCDVCC_MOS circuit	13
2002/4/1	0.9	Change pin name of SiS55X	5
		Change R332 and R333 resistance value of RTC circuit	30
		Change main power circuit	31
2002/6/20		modify SB1.8V circuit.	31

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Title: Revision History

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NOTE :

1 : FOR C/CB <= 0.1uF, USE 0603 SURFACE MOUNT CERAMIC CAPACITOR.

2 : FOR CB = 1uF, USE 0805 SURFACE MOUNT CERAMIC CAPACITOR.

3 : FOR CT = 10uF, USE 1206 SURFACE MOUNT SOLID TANTALUM CAPACITOR.

4 : FOR 1uF < CE < 22uF, USE DEEP SOLID TANTALUM CAPACITOR.

5 : FOR CE > 22uF, USE DEEP ALUMINUM ELECTROLYTIC CAPACITOR.

SILICON INTEGRATED SYSTEMS CORP.		
Title: Notes		
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MEMORY

55X-1

HOST

U13A
550-1

CPU FREQUENCY RATIO SELECT

	XBF1	XBF0
2.5	0	0
3	0	1
2(default)	1	0
Reserved	1	1

SILICON INTEGRATED SYSTEMS CORP.	
Title	550-1 (HOST/MEMORY)
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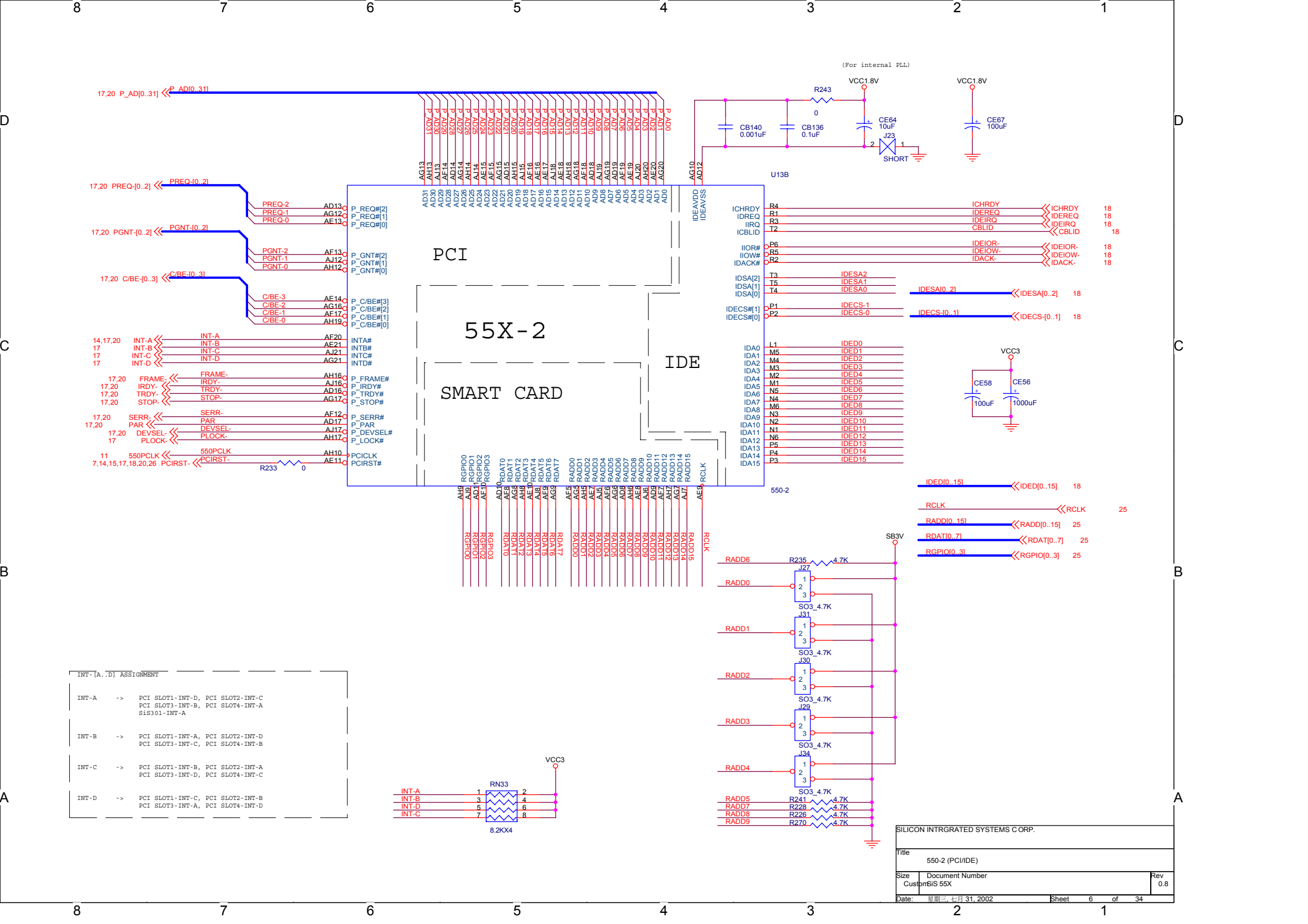
PCI
55X-2
IDE
SMART CARD
U13B
550-2
(For internal PLL)
VCC1.8V
R243
0
CB140
0.001uF
CB136
0.1uF
CE64
10uF
J23
SHORT
CE67
100uF
P_AD[0..31]
PREQ-[0..2]
PGNT-[0..2]
C/BE-[0..3]
INT-A
INT-B
INT-C
INT-D
FRAME-
IRDY-
TRDY-
STOP-
SERR-
PAR
DEVSEL-
PLOCK-
550PCLK
PCIRST-
R233
0
ICHRDY
IDEREQ
IDEIRQ
CBLID
IIOR#
IIOW#
IDACK#
IDSA[2]
IDSA[1]
IDSA[0]
IDECS#[1]
IDECS#[0]
IDEIOR-
IDEIOW-
IDACK-
IDESA2
IDESA1
IDESA0
IDECS-1
IDECS-0
IDESA[0..2]
IDECS-[0..1]
IDA0
IDA1
IDA2
IDA3
IDA4
IDA5
IDA6
IDA7
IDA8
IDA9
IDA10
IDA11
IDA12
IDA13
IDA14
IDA15
IDED0
IDED1
IDED2
IDED3
IDED4
IDED5
IDED6
IDED7
IDED8
IDED9
IDED10
IDED11
IDED12
IDED13
IDED14
IDED15
IDED[0..15]
RCLK
RADD[0..15]
RDAT[0..7]
RGPIO[0..3]
VCC3
CE58
100uF
CE56
1000uF
SB3V
RADD6
RADD0
RADD1
RADD2
RADD3
RADD4
RADD5
RADD7
RADD8
RADD9
R235
4.7K
J27
J31
J30
J29
J34
SO3_4.7K
R241
R228
R226
R270
RN33
8.2KX4
INT-[A..D] ASSIGNMENT
INT-A -> PCI SLOT1-INT-D, PCI SLOT2-INT-C
PCI SLOT3-INT-B, PCI SLOT4-INT-A
SiS301-INT-A
INT-B -> PCI SLOT1-INT-A, PCI SLOT2-INT-D
PCI SLOT3-INT-C, PCI SLOT4-INT-B
INT-C -> PCI SLOT1-INT-B, PCI SLOT2-INT-A
PCI SLOT3-INT-D, PCI SLOT4-INT-C
INT-D -> PCI SLOT1-INT-C, PCI SLOT2-INT-B
PCI SLOT3-INT-A, PCI SLOT4-INT-D
SILICON INTRGRATED SYSTEMS C ORP.
Title
550-2 (PCI/IDE)
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Custom
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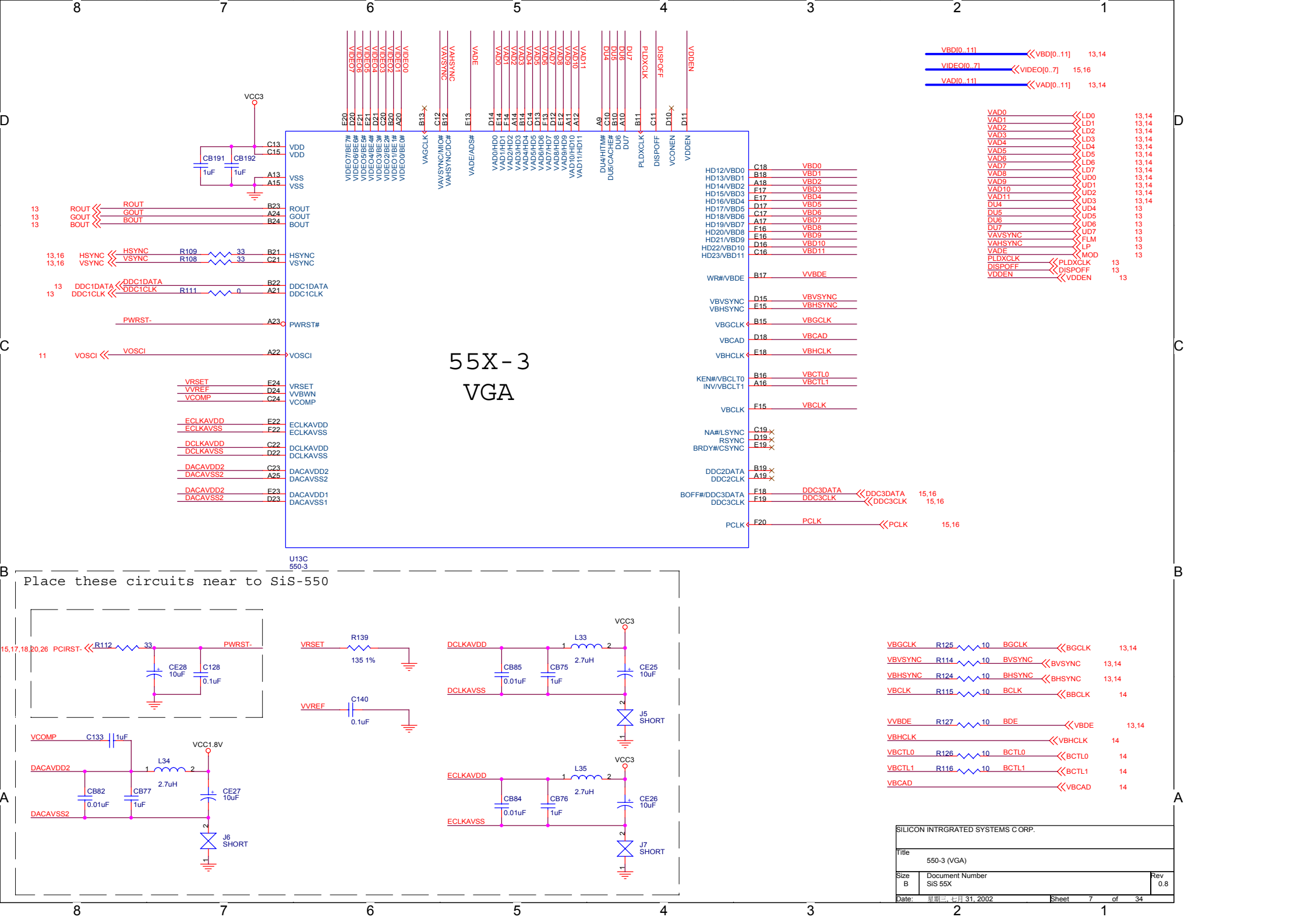
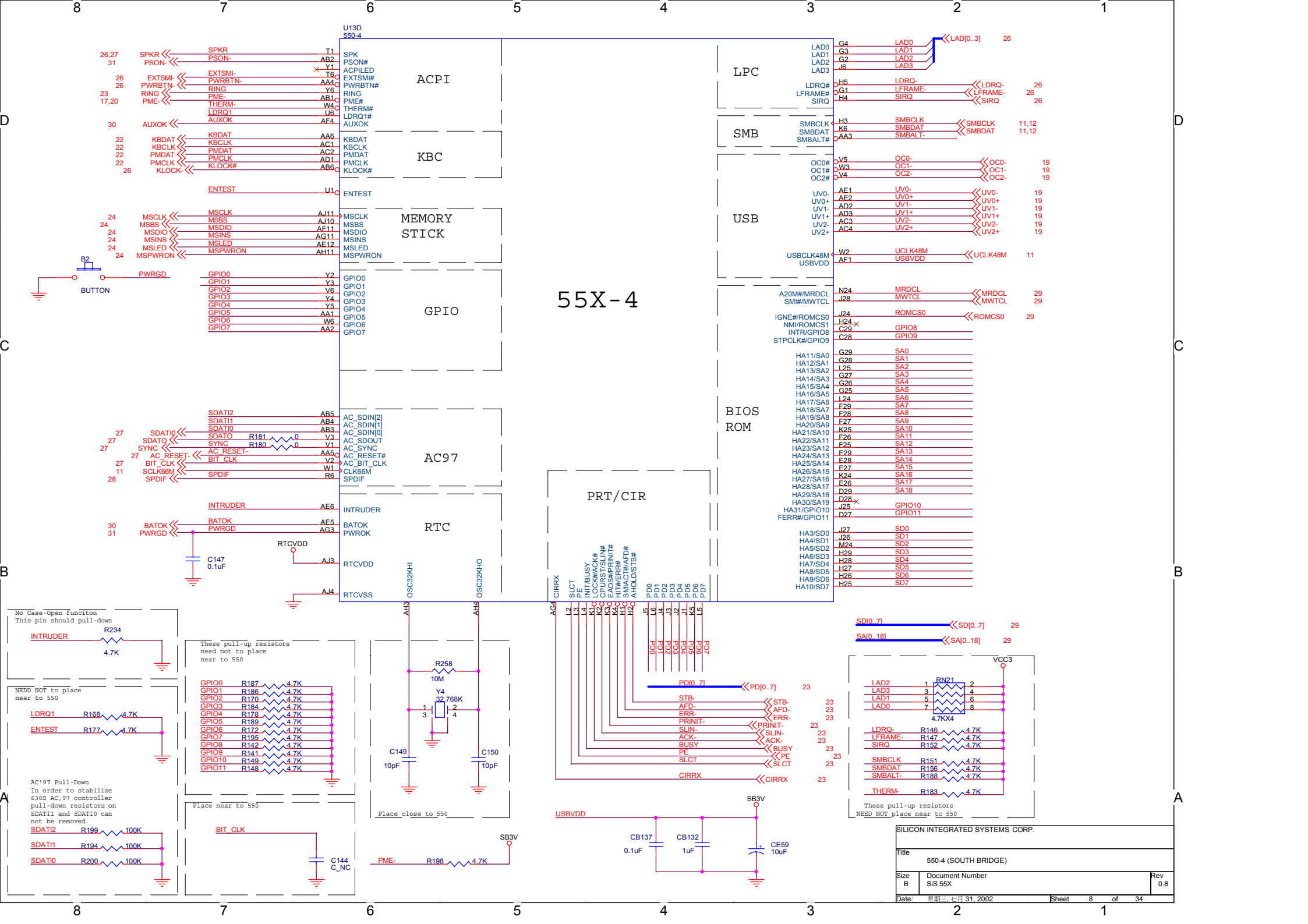
55X-3
VGA

U13C
550-3

Place these circuits near to SiS-550




U13D
550-4
55X-4
ACPI
KBC
MEMORY STICK
GPIO
AC97
RTC
PRT/CIR
LPC
SMB
USB
BIOS ROM
SPKR
PSON-
EXTSMI-
PWRBTN-
RING
PME-
THERM-
LDRQ1
AUXOK
KBDAT
KBCLK
PMDAT
PMCLK
KLOCK-
ENTEST
MSCLK
MSBS
MSDIO
MSINS
MSLED
MSPWRON
PWRGD
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
SDATI2
SDATI1
SDATI0
SDATO
SYNC
AC_RESET-
BIT_CLK
SCLK66M
SPDIF
INTRUDER
BATOK
PWRGD
RTCVDD
RTCVSS
OSC32KHI
OSC32KHO
LAD0
LAD1
LAD2
LAD3
LDRQ#
LFRAME#
SIRQ
SMBCLK
SMBDAT
SMBALT#
OC0#
OC1#
OC2#
UV0-
UV0+
UV1-
UV1+
UV2-
UV2+
USBCLK48M
USBVDD
A20M#/MRDCL
SMI#/MWTCL
IGNE#/ROMCS0
NMI/ROMCS1
INTR/GPIO8
STPCLK#/GPIO9
HA11/SA0
HA12/SA1
HA13/SA2
HA14/SA3
HA15/SA4
HA16/SA5
HA17/SA6
HA18/SA7
HA19/SA8
HA20/SA9
HA21/SA10
HA22/SA11
HA23/SA12
HA24/SA13
HA25/SA14
HA26/SA15
HA27/SA16
HA28/SA17
HA29/SA18
HA30/SA19
HA31/GPIO10
FERR#/GPIO11
HA3/SD0
HA4/SD1
HA5/SD2
HA6/SD3
HA7/SD4
HA8/SD5
HA9/SD6
HA10/SD7
CIRRX
SLCT
PE
INIT/BUSY
ACK#/ACK#
CPURST/SLIN#
EADS#/PRINIT#
HIT#/ERR#
SMIACT#/AFD#
AHOLD/STB#
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
B2
BUTTON
C147
0.1uF
C144
C_NC
C149
10pF
C150
10pF
R258
10M
Y4
32.768K
R234
4.7K
R181
R180
SB3V
USBVDD
CB137
0.1uF
CB132
1uF
CE59
10uF
VCC3
RN21
4.7KX4
SD[0..7]
SA[0..18]
LAD[0..3]
LDRQ-
LFRAME-
SIRQ
SMBCLK
SMBDAT
SMBALT-
OC0-
OC1-
OC2-
UV0-
UV0+
UV1-
UV1+
UV2-
UV2+
UCLK48M
MRDCL
MWTCL
ROMCS0
GPIO8
GPIO9
GPIO10
GPIO11
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
SA16
SA17
SA18
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
No Case-Open funciton
This pin should pull-down
NEDD NOT to place
near to 550
These pull-up resistors
need not to place
near to 550
AC'97 Pull-Down
In order to stabilize
630S AC,97 controller
pull-down resistors on
SDATI1 and SDATI0 can
not be removed.
Place near to 550
Place close to 550
These pull-up resistors
NEED NOT place near to 550
SILICON INTEGRATED SYSTEMS CORP.
Title
550-4 (SOUTH BRIDGE)
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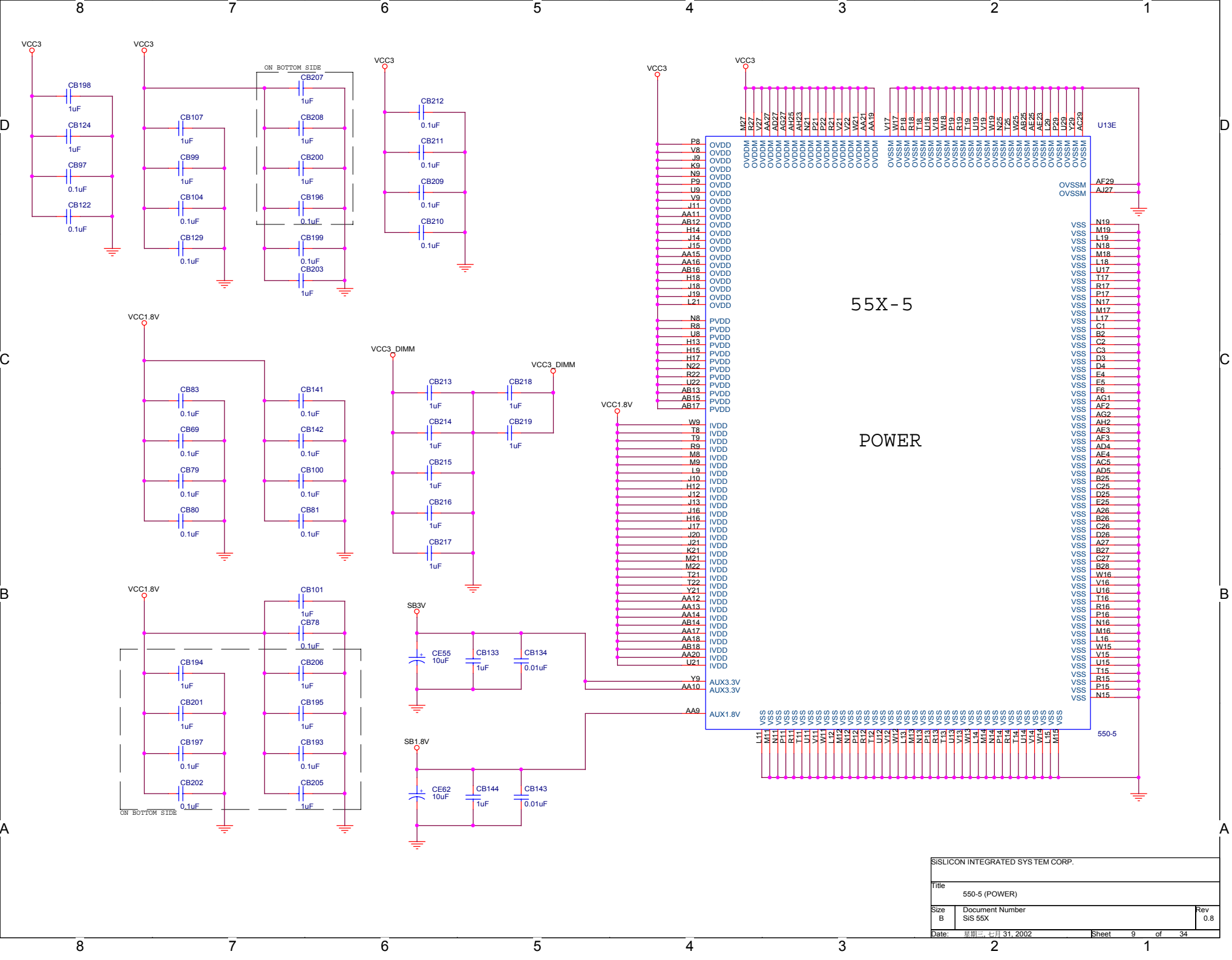

SISLICON INTEGRATED SYS TEM CORP.	
Title	550-5 (POWER)
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MD62: PCI Clock PLL Enable
0: Enable (Recommend)
1: Disable

MD61: SDRAM Clock DLL Enable
0: Enable (Recommend)
1: Disable

MD60: CPU Clock DLL Enable
0: Enable (Recommend)
1: Disable

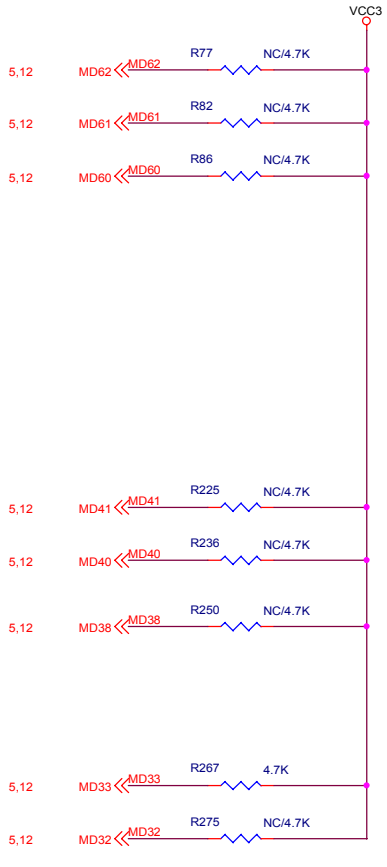
MD41: ROM interface select
0: Build-in ROM interface
1: Forward to LPC bus

MD40: Auto Restart
0: Disable
1: Enable

MD38: VGA Interrupt Function(INTA) Enable
0: Disable
1: Enable

MD33: Video Bridge Enable
0: Disable
1: Enable(302)

MD32: TV Type(PAL/NTSC) Select
0: Select NTSC system
1: Select PAL system



SILICON INTEGRATED SYSTEMS CORP.		
Title: 550 HARDWARE TRAP		
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Clock Generator

(5 OPTIONs)
1:ICS951901AF (ICS:default)
2:W83194BR-635 (WINBOND)
3:C9631 (IMI)
4:FS6227-01 (AMI)
5:W257 (ICWorks)

CLK1
CLOCK GEN

VCC3
L46
FB
CB185 0.1uF
CB182 0.1uF
CB184 0.1uF
CB183 0.1uF
CE80 22uF
CB163 0.001uF
CB174 0.001uF
CB162 0.001uF
CB161 0.001uF
VDDSDR
VDDREF
VDDSDR
VDDSDR
VDDSDR
VDD48
VDDAGP
VDDPCI
GNDREF
GND48
GNDAGP
GNDSDR
GNDSDR
GNDSDR
GNDPCI

VCC2.5V
L44
FB
CE73 22uF
CB166 0.1uF
CB167 0.001uF
CB168 0.1uF
CB165 0.001uF
VDDCPU
VDDCPU
GNDCPU

8,12 SMBCLK
8,12 SMBDAT
SMBCLK
SMBDAT
SCLK
SDATA

X1
X2
Y6
14.318MHz
C165 10pF
C166 10pF

CPU_C0
CPU_C1
CPUCS_C2
FS1/PCICLK_F
FS2/PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5
FS3/REF0
AGPSEL/REF1
MODE/24_48MHZ
FS0/48MHZ
CPUSTP#/SDRAM11
PCISTP#/SDRAM10
SDRSTOP#/SDRAM9
PD#/SDRAM8
SDRAM7
SDRAM6
SDRAM5
SDRAM4
SDRAM3
SDRAM2
SDRAM1
SDRAM0
SDRAM12
AGPCLK1
AGPCLK0

Damping Resistors
Place near to the
Clock Generator

R283 22 R1CPUCLK → R1CPUCLK 5
R284 22 R1CPUCLKBY → R1CPUCLKBY 5
R285 22 550CCLK → 550CCLK 5
R311 33 FS1 550PCLK → 550PCLK 6
R312 33 PCICLK1 → PCICLK1 17
R313 33 PCICLK2 → PCICLK2 17
R314 33 PCICLK → PCICLK 26
R315 33 900PCLK → 900PCLK 20
R310 33 FS3 VOSCI → VOSCI 7
R318 33 SEL VBRCLK → VBRCLK 14
R317 22 FS0 UCLK48M → UCLK48M 8
R289 22 SDCLK3
R288 22 SDCLK2
R287 22 SDCLK1
R286 22 SDCLK0
R290 22 550DCLK → 550DCLK 5
R316 22 SCLK66M → SCLK66M 8
SDCLK[0..3] → SDCLK[0..3] 12

By-Pass Capacitors
Place near to the Clock Gernerator

R1CPUCLK C153 10pF
R1CPUCLKBY C154 10pF
550CCLK C155 10pF
550PCLK C167 10pF
PCICLK1 C168 10pF
PCICLK2 C169 10pF
PCICLK C170 10pF
900PCLK C171 10pF
VOSCI C164 10pF
VBRCLK C163 10pF
UCLK48M C173 10pF
SDCLK3 C159 10pF
SDCLK2 C158 10pF
SDCLK1 C157 10pF
SDCLK0 C156 10pF
550DCLK C160 10pF
SCLK66M C172 10pF

VCC2.5V
CE77 22uF
CB170 0.1uF
CB169 0.001uF

VCC3
CE84 22uF
CB175 0.1uF
CB178 0.001uF

VCC3
Frequency Selection
JP16
R309 2.7K
JUMPER
SEL

JP17
R329 2.7K FS0
R328 2.7K FS1
R327 2.7K FS2
R326 2.7K FS3
HEASER 4X2

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Title	CLOCK GENERATOR	
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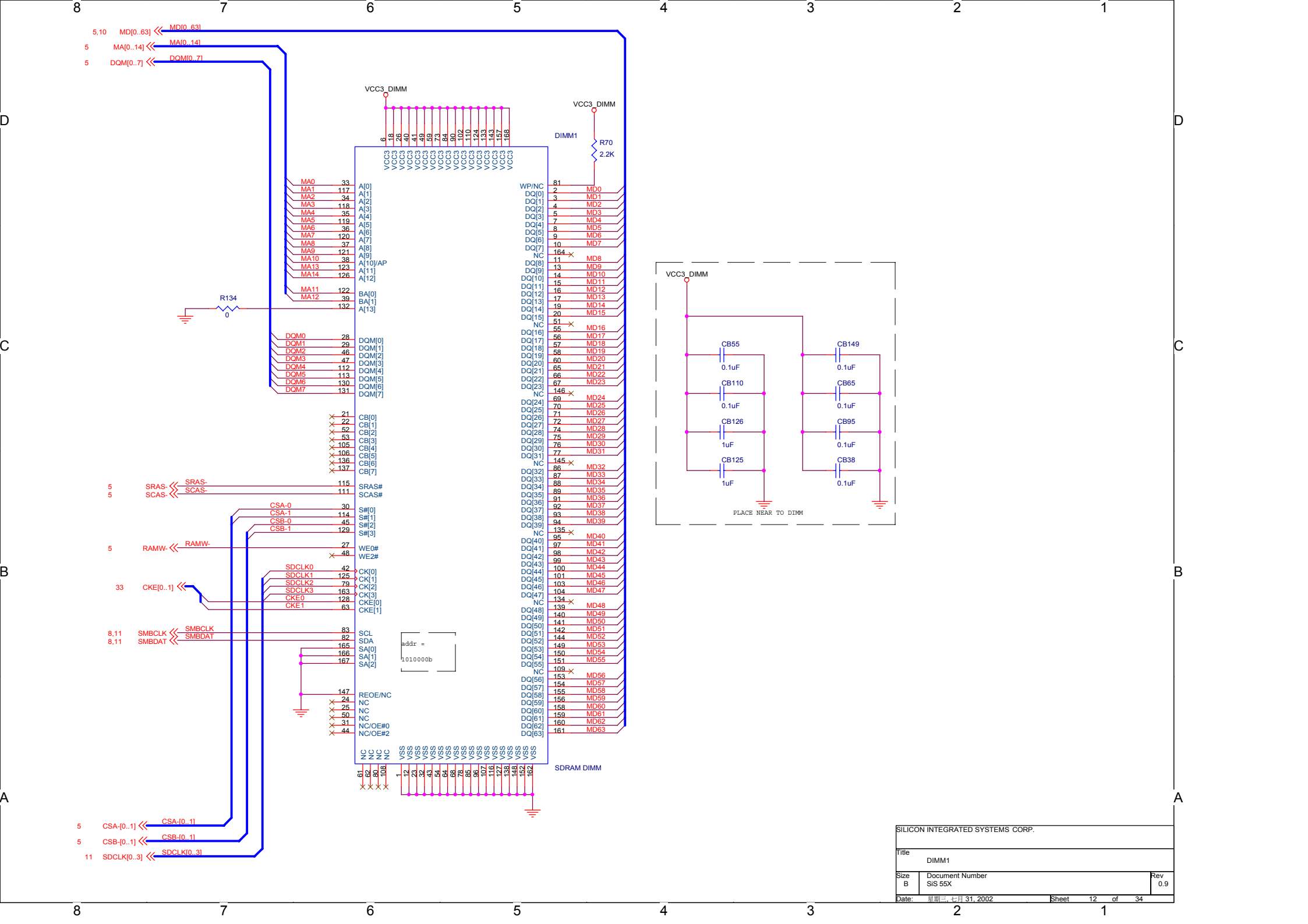

SILICON INTEGRATED SYSTEMS CORP.		
Title: DIMM1		
Size: B	Document Number: SiS 55X	Rev: 0.9
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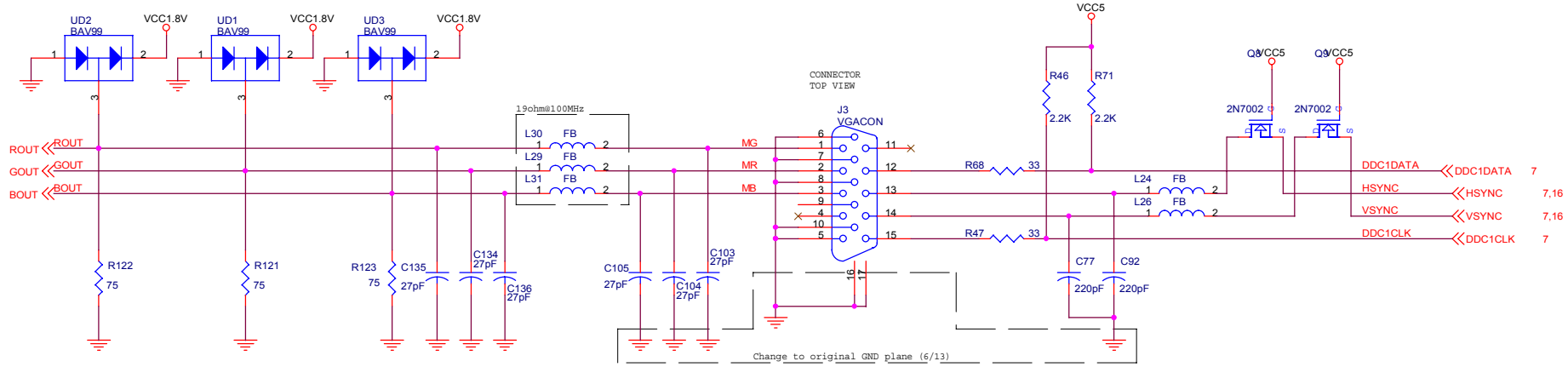
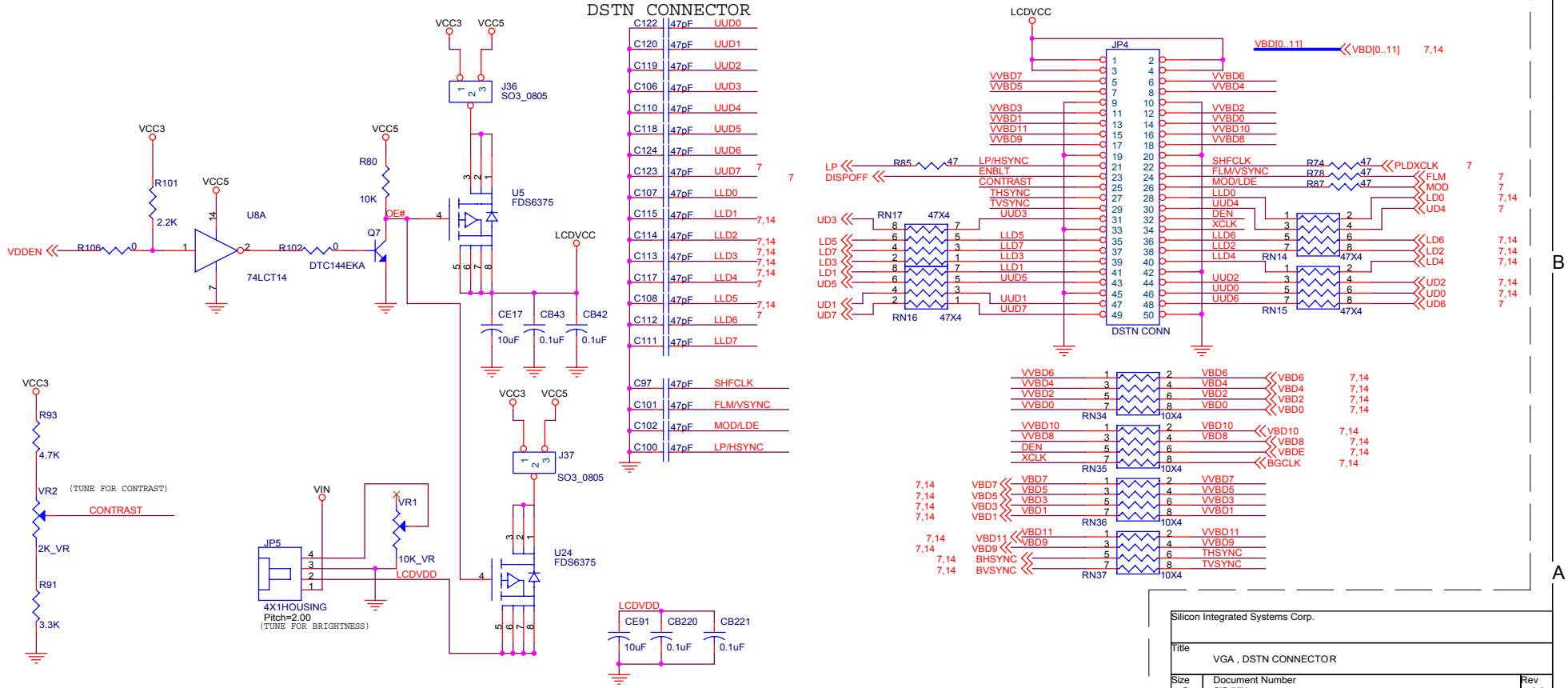
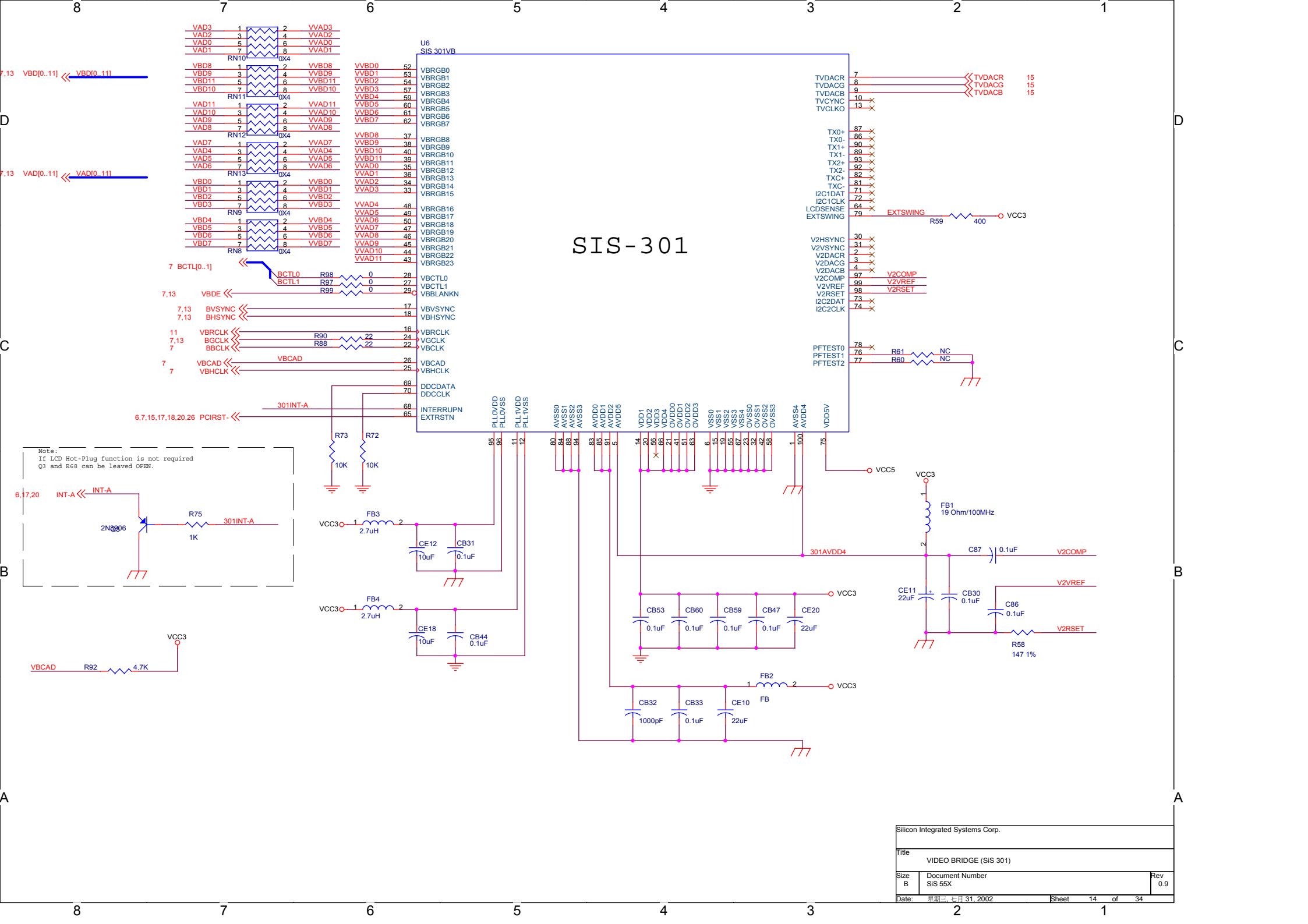
VGA CONNECTOR



DSTN CONNECTOR



Silicon Integrated Systems Corp.		
Title: VGA , DSTN CONNECTOR		
Size: Custom	Document Number: SiS 55X	Rev: 0.9
Date: 星期三, 七月 31, 2002	Sheet 13 of 34	


SIS-301
U6
SIS 301VB
Note:
If LCD Hot-Plug function is not required
Q3 and R68 can be leaved OPEN.
Silicon Integrated Systems Corp.
Title
VIDEO BRIDGE (SiS 301)
Size
B
Document Number
SiS 55X
Rev
0.9
Date:
星期二, 七月 31, 2002
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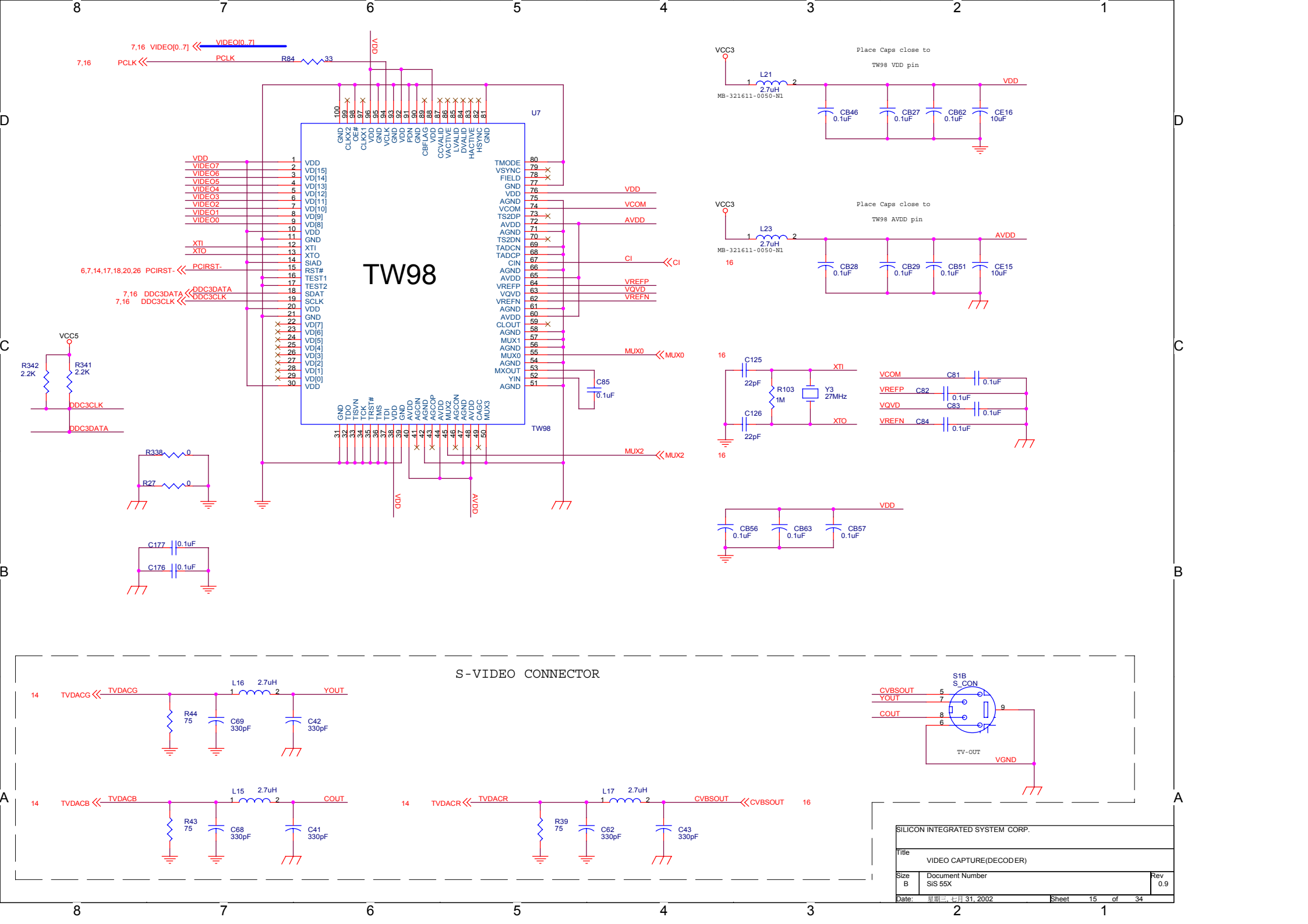
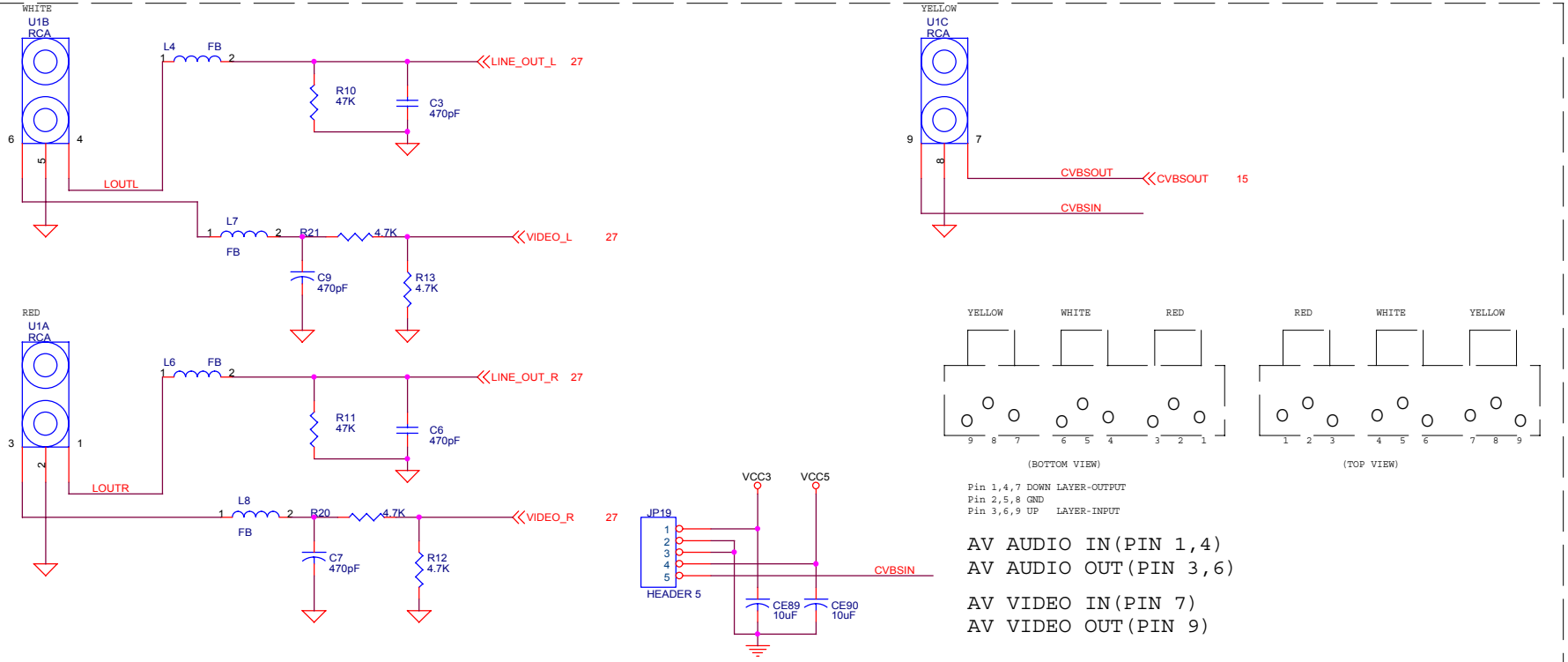
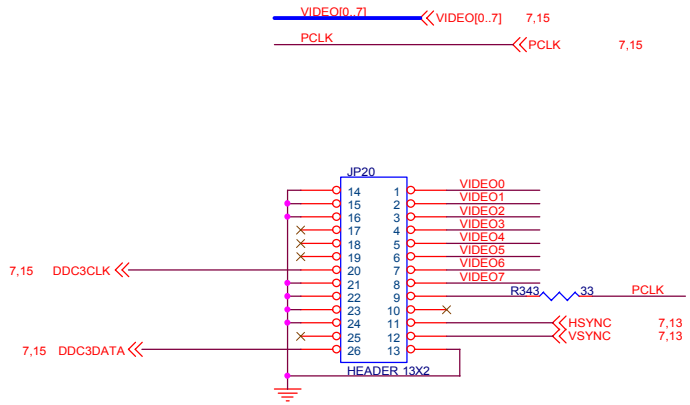


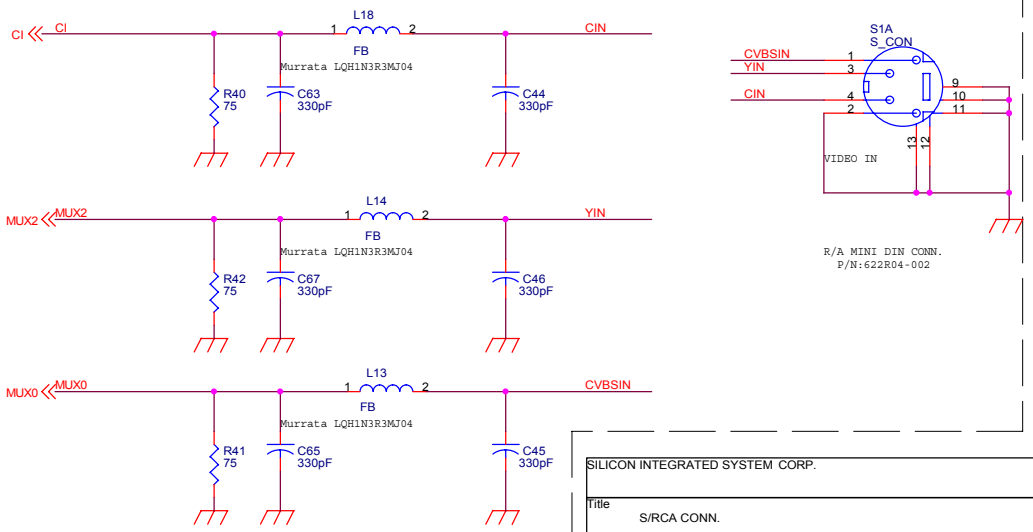
SILICON INTEGRATED SYSTEM CORP.	
Title	VIDEO CAPTURE(DECODER)
Size B	Document Number SiS 55X
Rev	0.9
Date:	星期三, 七月 31, 2002
Sheet	15 of 34



FEATURE CONN

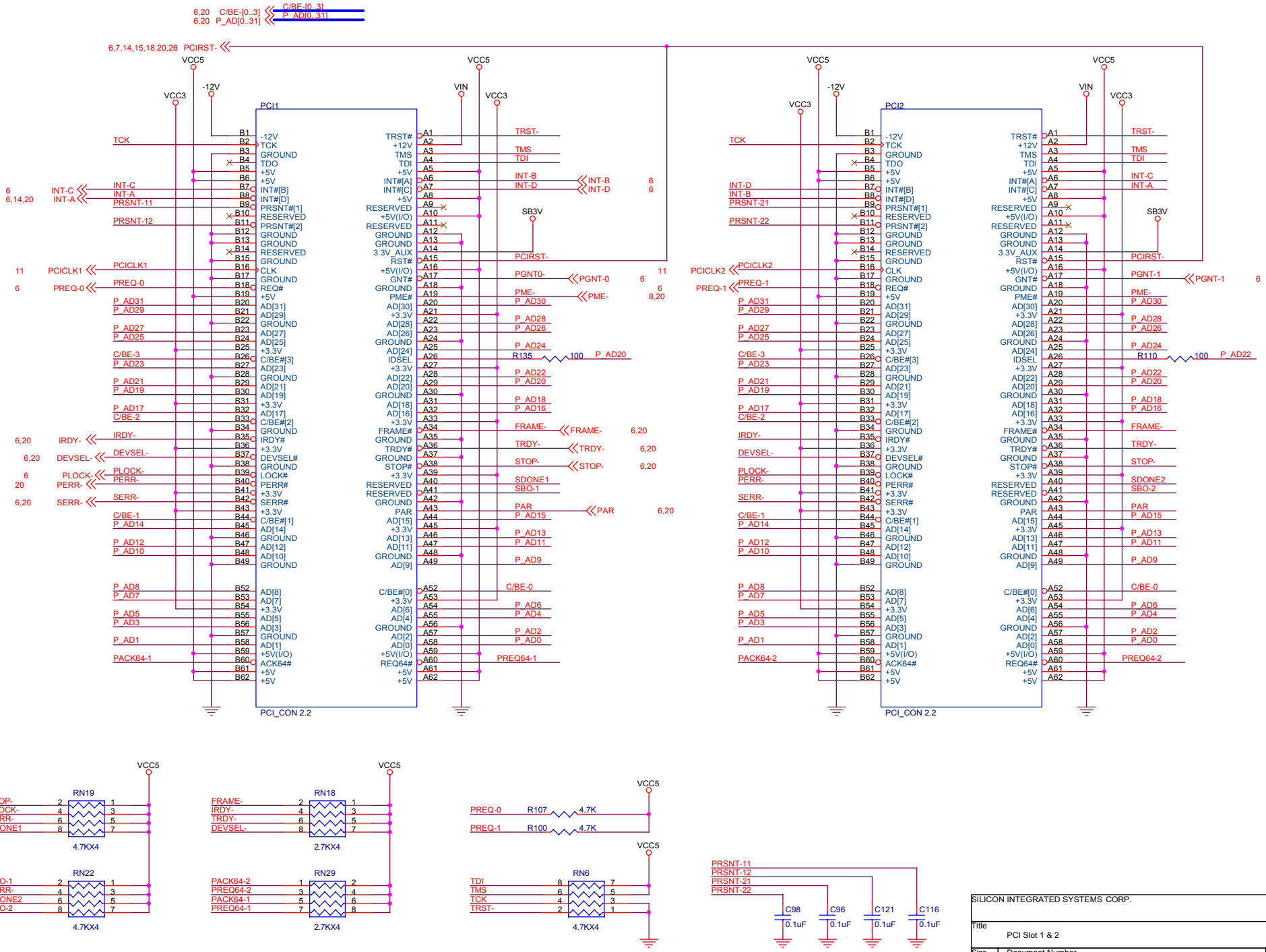


S-VIDEO CONNECTOR

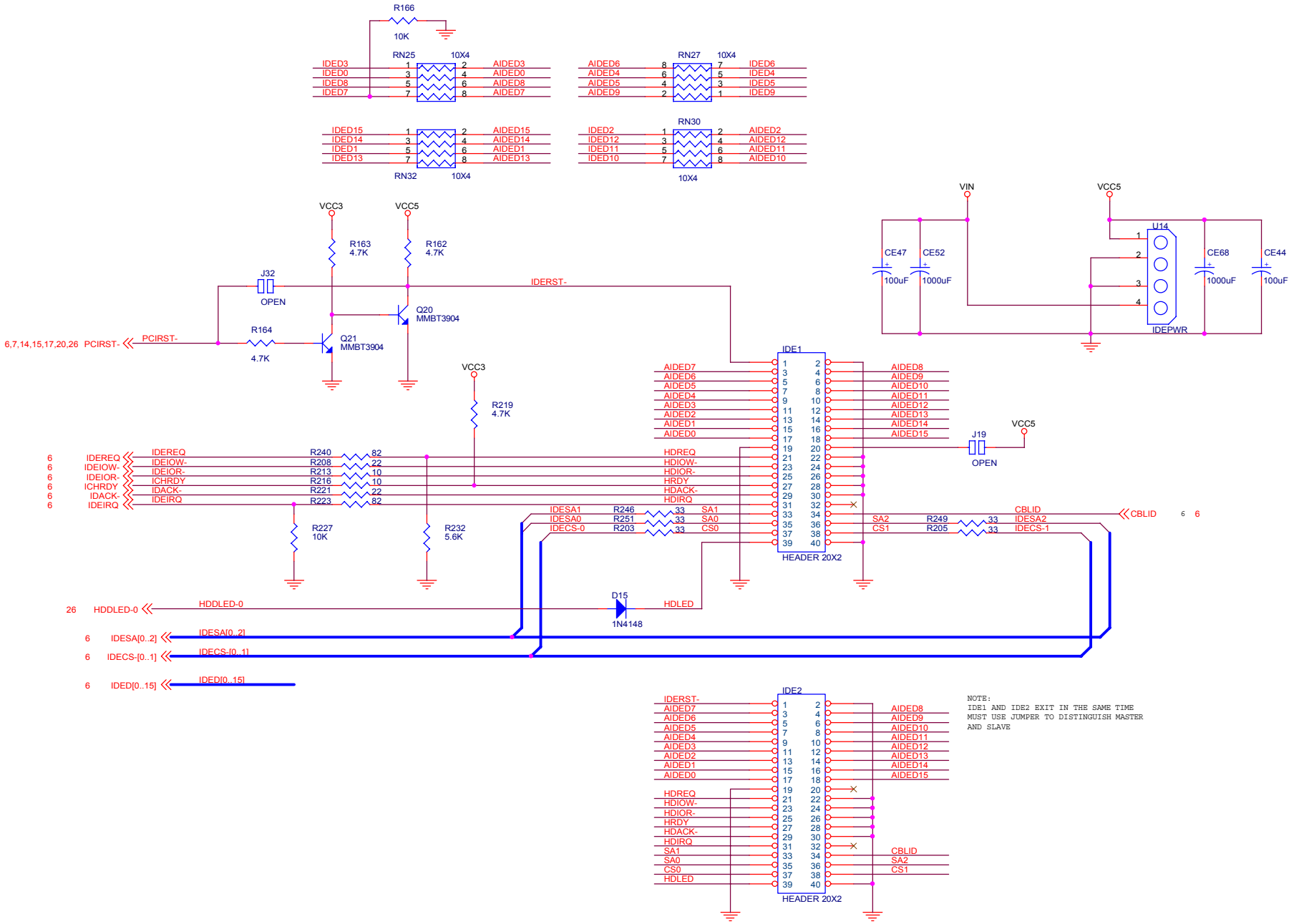


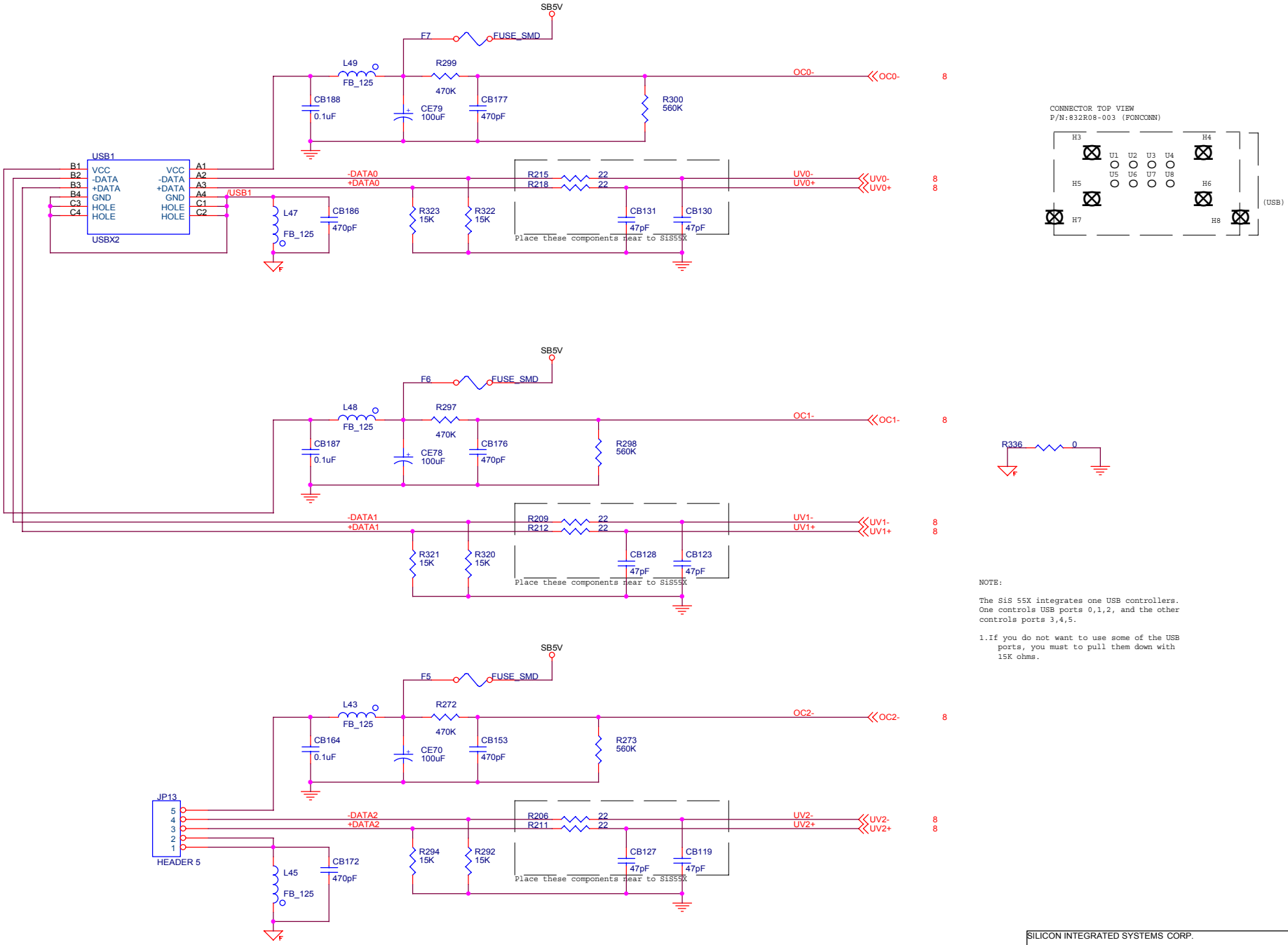
SILICON INTEGRATED SYSTEM CORP.		
Title: S/RCA CONN.		
Size: B	Document Number: SiS 55X	Rev: 0.9
Date: 星期三, 七月 31, 2002	Sheet 16 of 34	

PCI Slot 1 & 2



SILICON INTEGRATED SYSTEMS CORP.		
Title: PCI Slot 1 & 2		
Size: Custom	Document Number: SiS 55X	Rev: 0.9
Date: 星期三, 七月 31, 2002	Sheet 17 of 34	


R166
10K
RN25 10X4
IDED3 IDED0 IDED8 IDED7
AIDED3 AIDED0 AIDED8 AIDED7
RN27 10X4
AIDED6 AIDED4 AIDED5 AIDED9
IDED6 IDED4 IDED5 IDED9
RN32 10X4
IDED15 IDED14 IDED1 IDED13
AIDED15 AIDED14 AIDED1 AIDED13
RN30 10X4
IDED2 IDED12 IDED11 IDED10
AIDED2 AIDED12 AIDED11 AIDED10
VIN
VCC5
U14
IDEPWR
CE47 100uF
CE52 1000uF
CE68 1000uF
CE44 100uF
VCC3
VCC5
R163 4.7K
R162 4.7K
J32
OPEN
IDERST-
Q20 MMBT3904
Q21 MMBT3904
R164 4.7K
6,7,14,15,17,20,26 PCIRST-
PCIRST-
VCC3
R219 4.7K
IDE1
HEADER 20X2
AIDED7 AIDED6 AIDED5 AIDED4 AIDED3 AIDED2 AIDED1 AIDED0
AIDED8 AIDED9 AIDED10 AIDED11 AIDED12 AIDED13 AIDED14 AIDED15
J19
OPEN
VCC5
6 IDEREQ
6 IDEIOW-
6 IDEIOR-
6 ICHRDY
6 IDACK-
6 IDEIRQ
IDEREQ R240 82 HDREQ
IDEIOW- R208 22 HDIOW-
IDEIOR- R213 10 HDIOR-
ICHRDY R216 10 HRDY
IDACK- R221 22 HDACK-
IDEIRQ R223 82 HDIRQ
R227 10K
R232 5.6K
IDESA1 R246 33 SA1
IDESA0 R251 33 SA0
IDECS-0 R203 33 CS0
SA2 R249 33 IDESA2
CS1 R205 33 IDECS-1
CBLID
CBLID 6 6
26 HDDLED-0
HDDLED-0
D15
1N4148
HDLED
6 IDESA[0..2]
IDESA[0..2]
6 IDECS-[0..1]
IDECS-[0..1]
6 IDED[0..15]
IDED[0..15]
IDE2
HEADER 20X2
IDERST- AIDED7 AIDED6 AIDED5 AIDED4 AIDED3 AIDED2 AIDED1 AIDED0
AIDED8 AIDED9 AIDED10 AIDED11 AIDED12 AIDED13 AIDED14 AIDED15
HDREQ HDIOW- HDIOR- HRDY HDACK- HDIRQ SA1 SA0 CS0 HDLED
CBLID SA2 CS1
NOTE:
IDE1 AND IDE2 EXIT IN THE SAME TIME
MUST USE JUMPER TO DISTINGUISH MASTER
AND SLAVE
NOTE:
SIS IS NOT RESPONSIBLE FOR
ANY ERRORS OR OMISSIONS IN
THESE SCHEMATICS. THIS IS
AN EXAMPLE ONLY.
SILICON INTEGRATED SYSTEMS CORP.
Title
IDE CONNECTORS
Size Custom
Document Number SiS 55X
Rev 0.9
Date: 星期三, 七月 31, 2002
Sheet 18 of 34


SB5V
F7
FUSE_SMD
L49
FB_125
R299
470K
CB188
0.1uF
CE79
100uF
CB177
470pF
R300
560K
OC0-
OC0-
USB1
B1 VCC
B2 -DATA
B3 +DATA
B4 GND
C3 HOLE
C4 HOLE
VCC A1
-DATA A2
+DATA A3
GND A4
HOLE C1
HOLE C2
USBX2
/USB1
-DATA0
+DATA0
L47
FB_125
CB186
470pF
R323
15K
R322
15K
R215
R218
22
22
UV0-
UV0+
CB131
47pF
CB130
47pF
Place these components near to SiS55X
SB5V
F6
FUSE_SMD
L48
FB_125
R297
470K
CB187
0.1uF
CE78
100uF
CB176
470pF
R298
560K
OC1-
OC1-
-DATA1
+DATA1
R209
R212
22
22
UV1-
UV1+
R321
15K
R320
15K
CB128
47pF
CB123
47pF
Place these components near to SiS55X
SB5V
F5
FUSE_SMD
L43
FB_125
R272
470K
CB164
0.1uF
CE70
100uF
CB153
470pF
R273
560K
OC2-
OC2-
JP13
5
4
3
2
1
HEADER 5
-DATA2
+DATA2
L45
FB_125
CB172
470pF
R294
15K
R292
15K
R206
R211
22
22
UV2-
UV2+
CB127
47pF
CB119
47pF
Place these components near to SiS55X
CONNECTOR TOP VIEW
P/N:832R08-003 (FONCONN)
H3
H4
U1 U2 U3 U4
U5 U6 U7 U8
H5
H6
H7
H8
(USB)
R336
0
NOTE:
The SiS 55X integrates one USB controllers.
One controls USB ports 0,1,2, and the other
controls ports 3,4,5.
1.If you do not want to use some of the USB
ports, you must to pull them down with
15K ohms.
SILICON INTEGRATED SYSTEMS CORP.
Title
USB CONNECTORS
Size
Custom
Document Number
SiS 55X
Rev
0.8
Date:
星期三, 七月 31, 2002
Sheet
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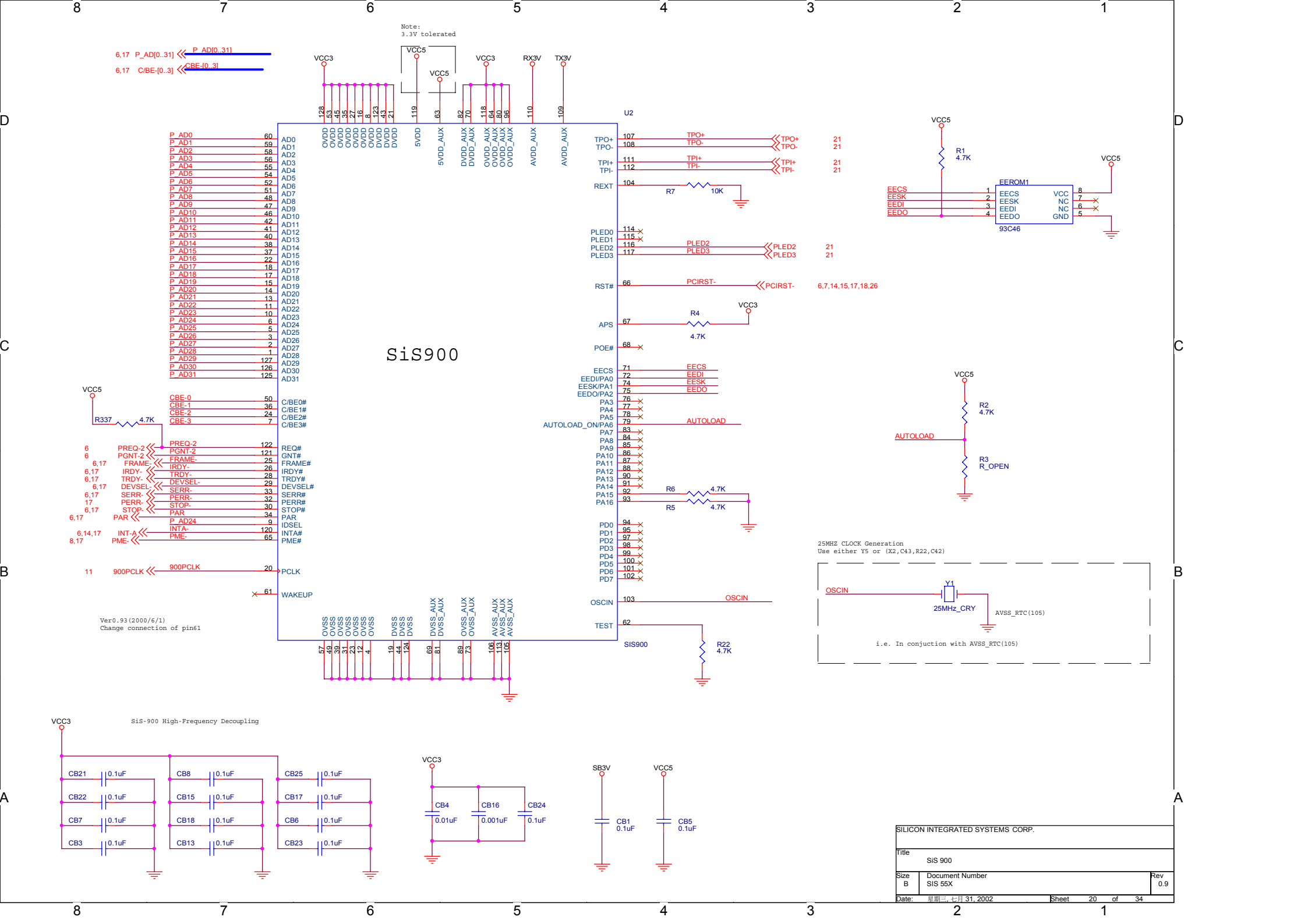
of
34


Note:
3.3V tolerated
SiS900
U2
SIS900
Ver0.93(2000/6/1)
Change connection of pin61
25MHZ CLOCK Generation
Use either Y5 or (X2,C43,R22,C42)
i.e. In conjuction with AVSS_RTC(105)
SiS-900 High-Frequency Decoupling
EEROM1
93C46
SILICON INTEGRATED SYSTEMS CORP.
Title
SiS 900
Size
B
Document Number
SIS 55X
Rev
0.9
Date:
星期三, 七月 31, 2002
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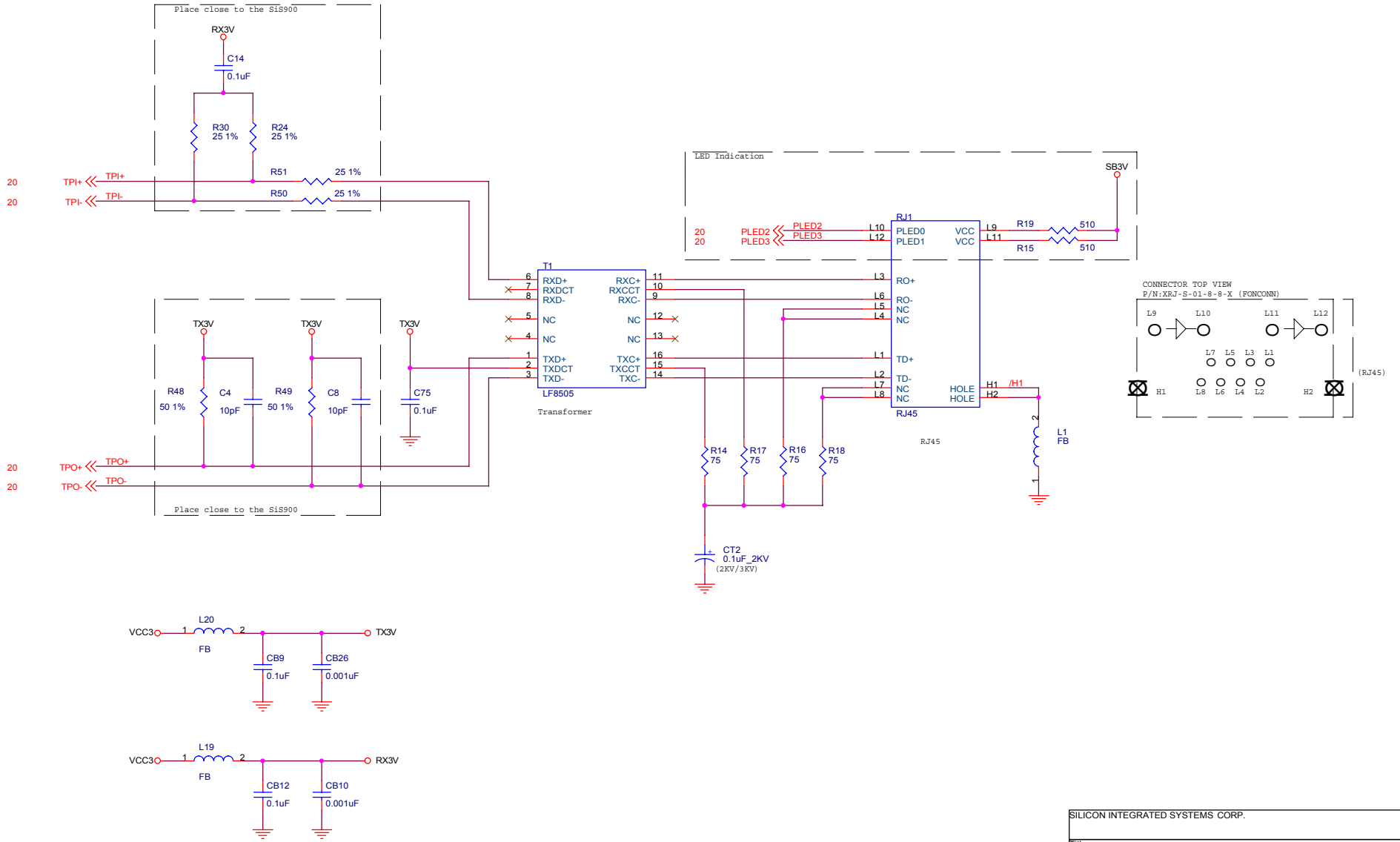
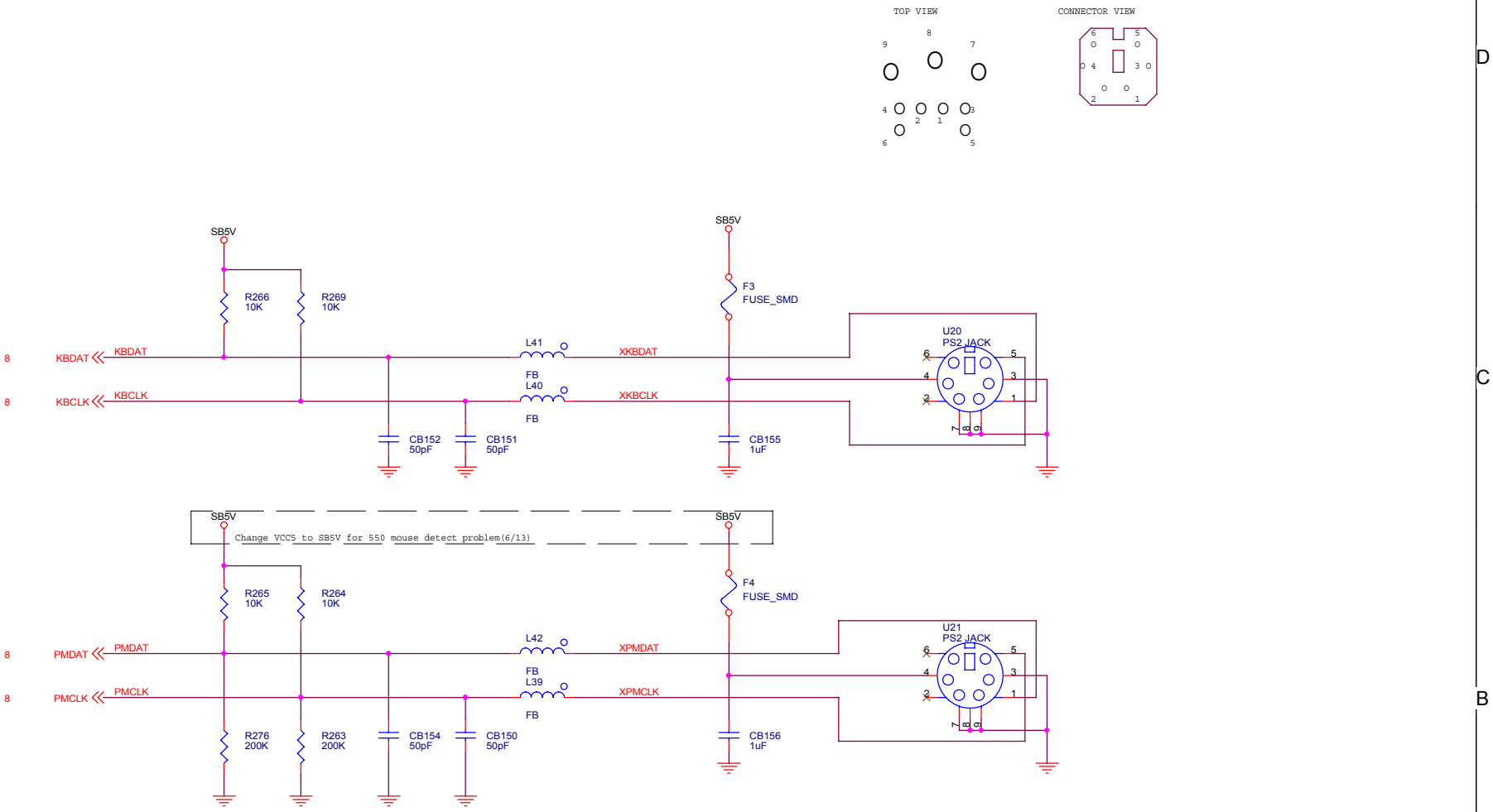
34

RJ45 Connector

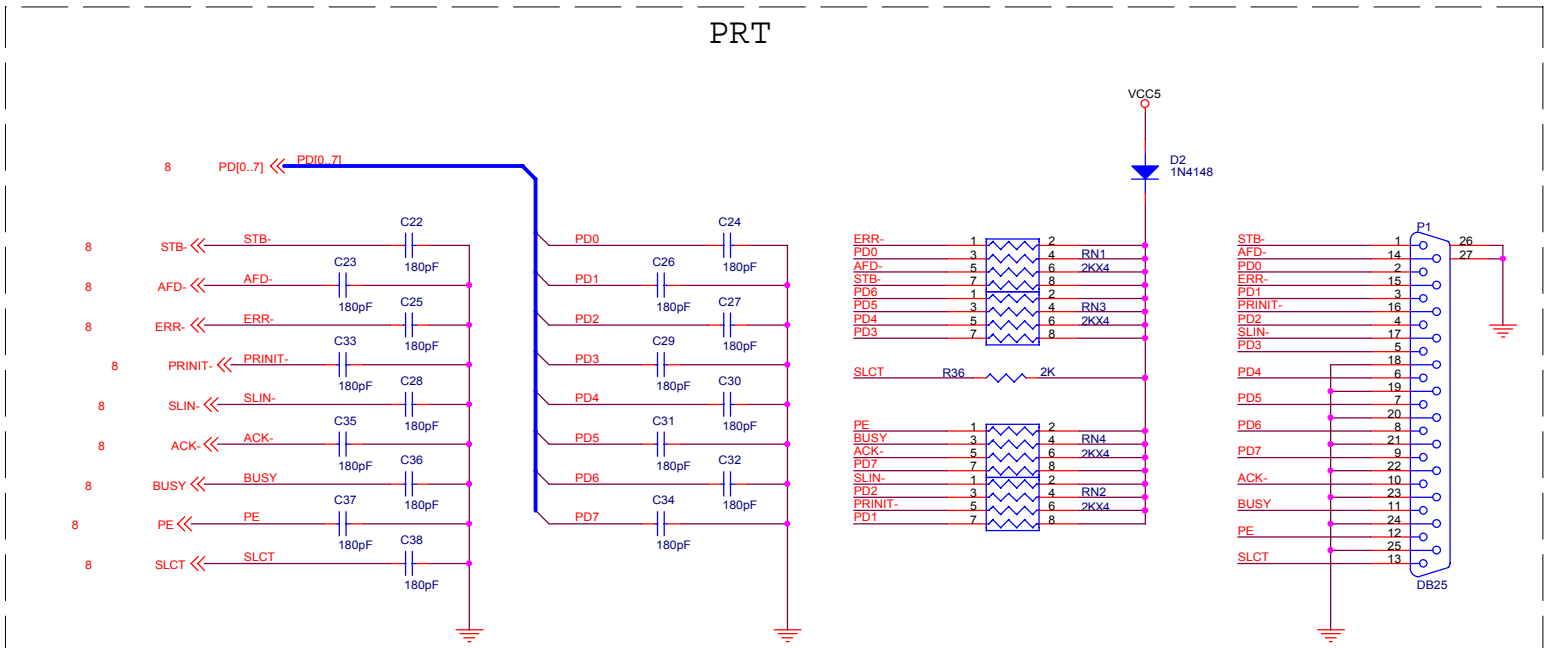


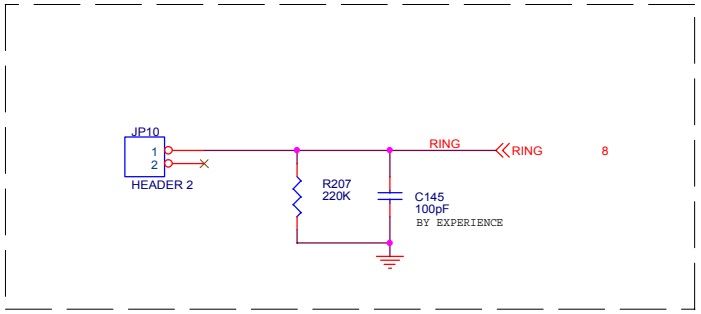
SILICON INTEGRATED SYSTEMS CORP.		
Title: RJ45 Connector		
Size: B	Document Number: SiS 55X	Rev: 0.9
Date: 星期三, 七月 31, 2002	Sheet 21 of 34	

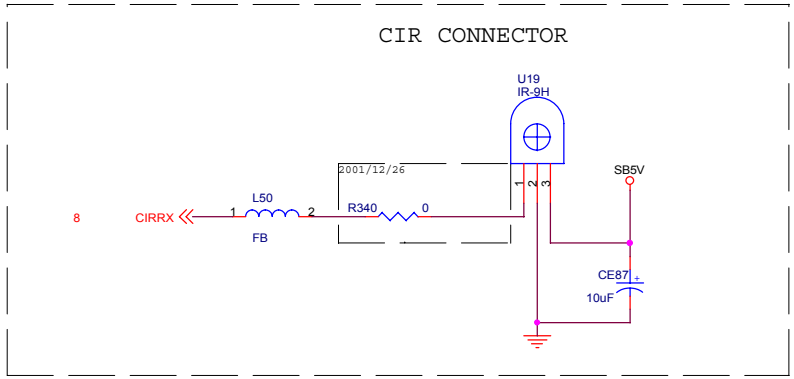


NOTE:
SIS IS NOT RESPONSIBLE FOR ANY ERRORS OR OMISSIONS IN THESE SCHEMATICS. THIS IS AN EXAMPLE ONLY.

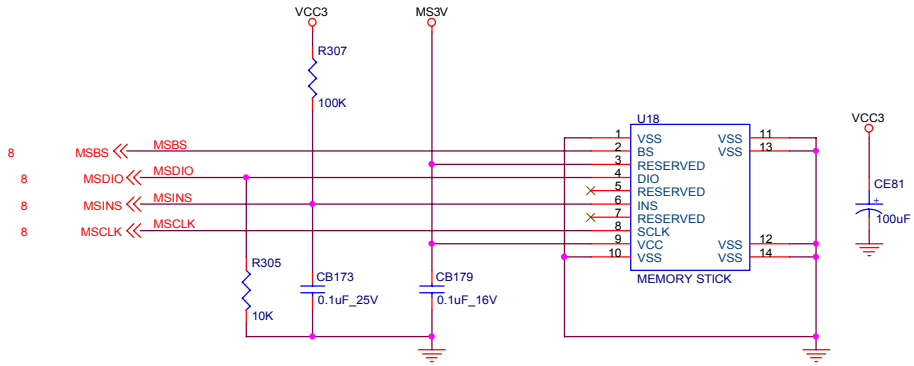
SILICON INTEGRATED SYSTEMS CORP.		
Title: KEYBOARD & MOUSE CONNECTORS		
Size: B	Document Number: SiS 55X	Rev: 0.9
Date: 星期三, 七月 31, 2002	Sheet 22 of 34	

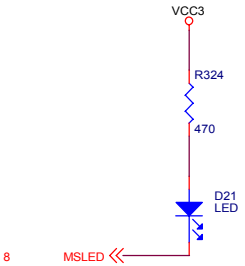


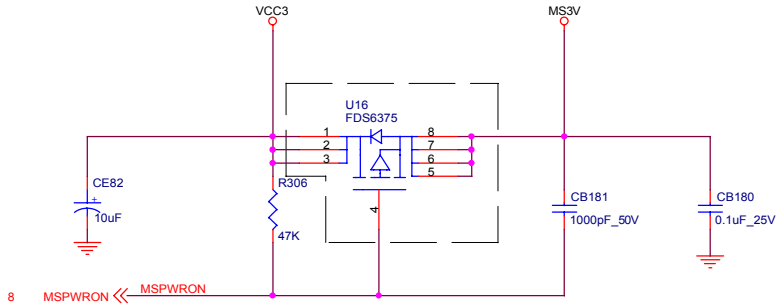




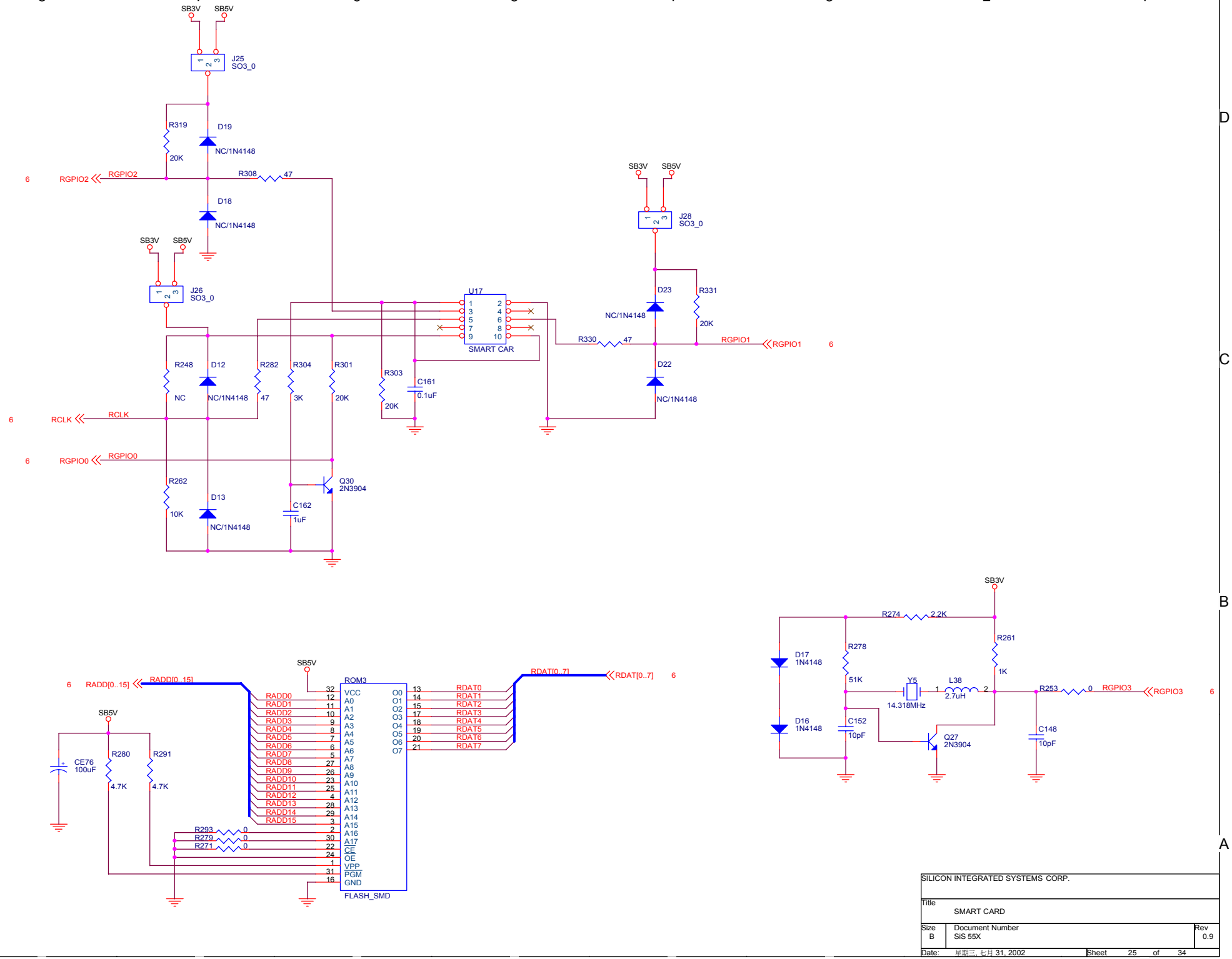
SILICON INTEGRATED SYSTEMS CORP.		
Title: PRT/CIR		
Size: B	Document Number: SiS 55X	Rev: 0.9
Date: 星期三, 七月 31, 2002	Sheet 23 of 34	



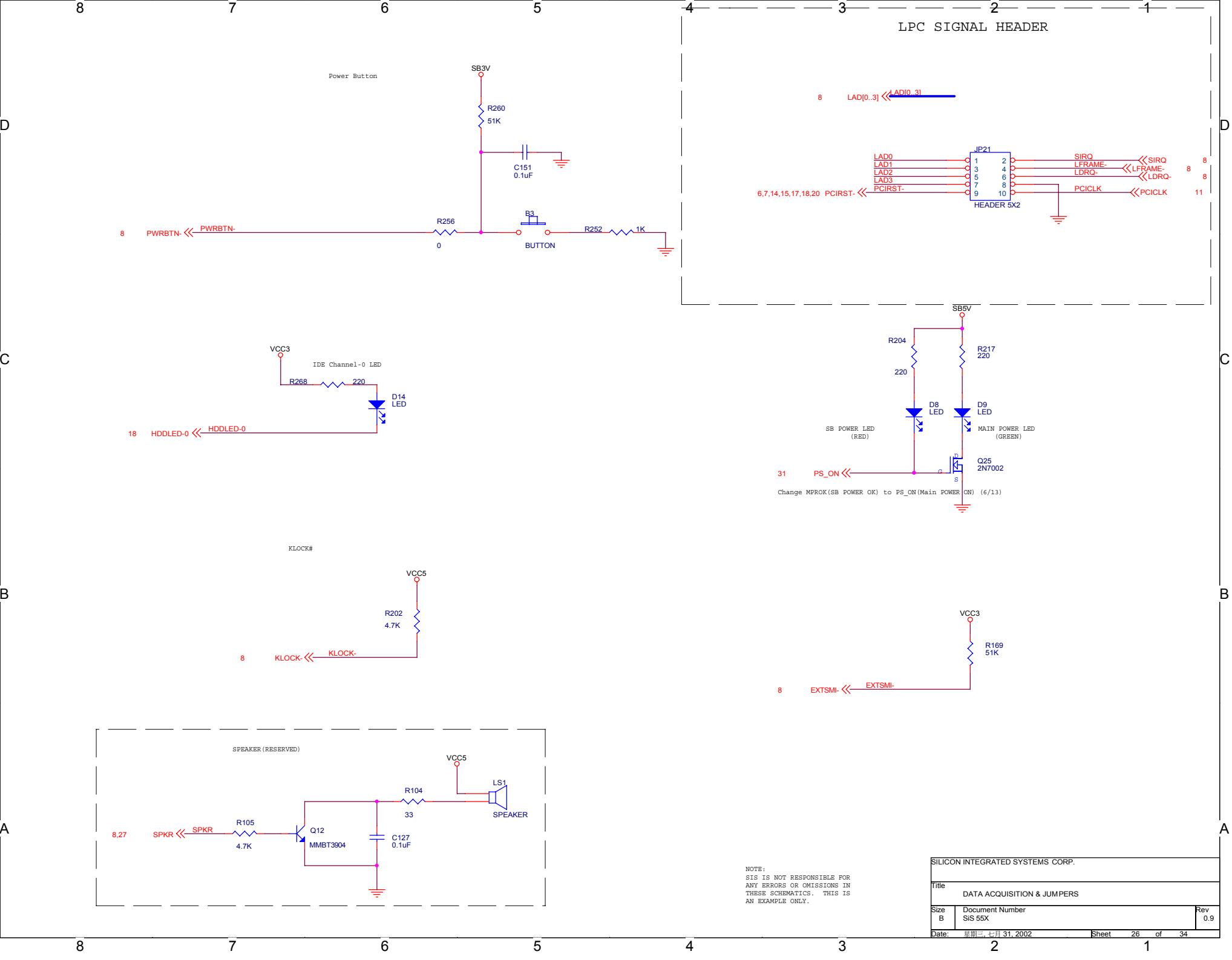




SILICON INTEGRATED SYSTEMS CORP.		
Title: MEMORY STICK		
Size: B	Document Number: SiS 55X	Rev: 0.9
Date: 星期三, 七月 31, 2002	Sheet 24 of 34	



SILICON INTEGRATED SYSTEMS CORP.		
Title: SMART CARD		
Size: B	Document Number: SiS 55X	Rev: 0.9
Date: 星期三, 七月 31, 2002	Sheet 25 of 34	


LPC SIGNAL HEADER
Power Button
SB3V
R260
51K
C151
0.1uF
R256
0
B3
BUTTON
R252
1K
8
PWRBTN-
PWRBTN-
LAD[0..3]
LAD[0..3]
JP21
LAD0
LAD1
LAD2
LAD3
PCIRST-
6,7,14,15,17,18,20 PCIRST-
SIRQ
LFRAME-
LDRQ-
PCICLK
HEADER 5X2
SIRQ
LFRAME-
LDRQ-
PCICLK
11
VCC3
IDE Channel-0 LED
R268
220
D14
LED
18
HDDLED-0
HDDLED-0
SB5V
R204
220
R217
220
D8
LED
D9
LED
SB POWER LED
(RED)
MAIN POWER LED
(GREEN)
Q25
2N7002
31
PS_ON
Change MPROK(SB POWER OK) to PS_ON(Main POWER ON) (6/13)
KLOCK#
VCC5
R202
4.7K
8
KLOCK-
KLOCK-
VCC3
R169
51K
8
EXTSMI-
EXTSMI-
SPEAKER(RESERVED)
VCC5
R104
33
LS1
SPEAKER
8,27
SPKR
SPKR
R105
4.7K
Q12
MMBT3904
C127
0.1uF
NOTE:
SIS IS NOT RESPONSIBLE FOR
ANY ERRORS OR OMISSIONS IN
THESE SCHEMATICS. THIS IS
AN EXAMPLE ONLY.
SILICON INTEGRATED SYSTEMS CORP.
Title
DATA ACQUISITION & JUMPERS
Size
B
Document Number
SiS 55X
Rev
0.9
Date:
星期三, 七月 31, 2002
Sheet
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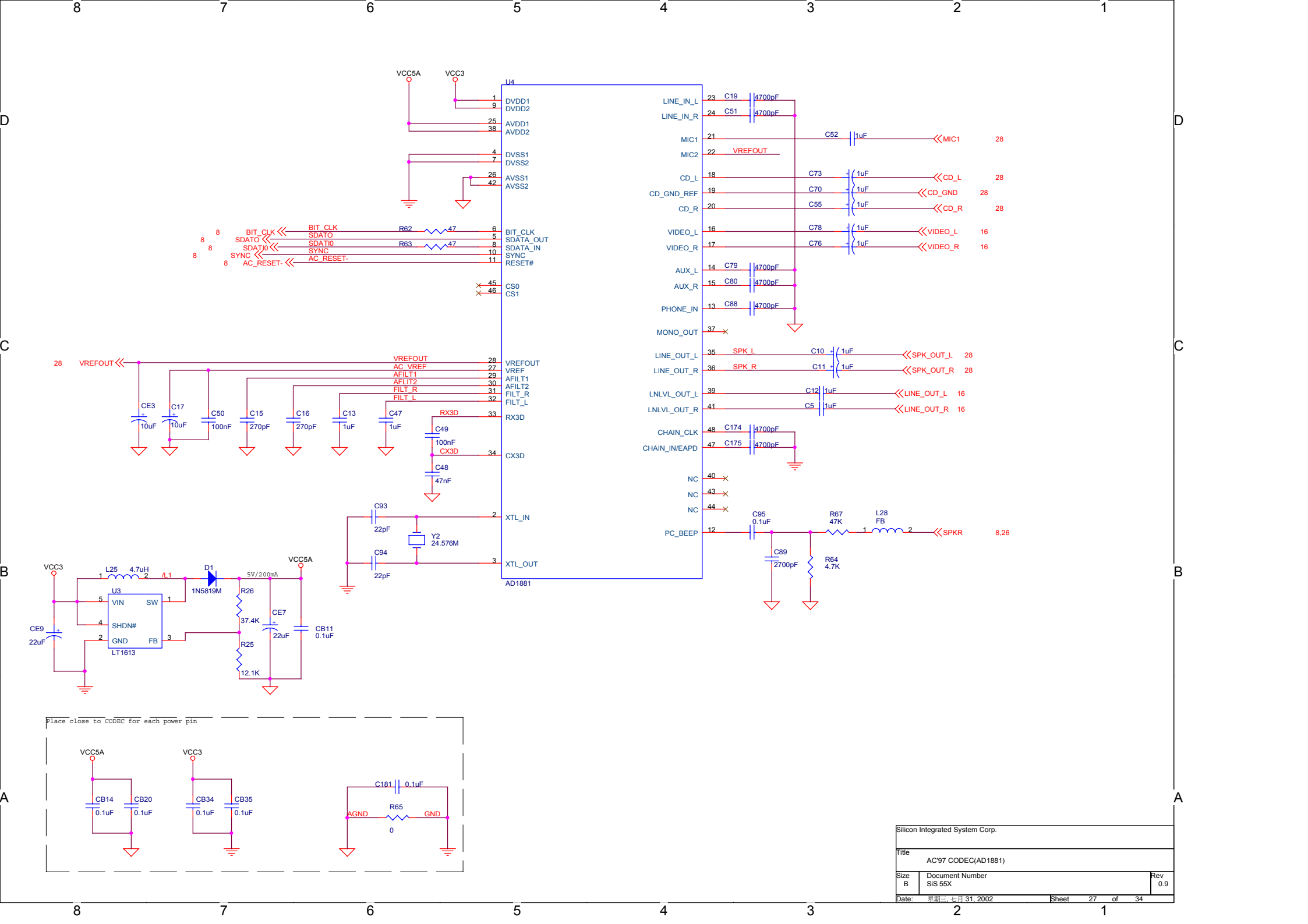
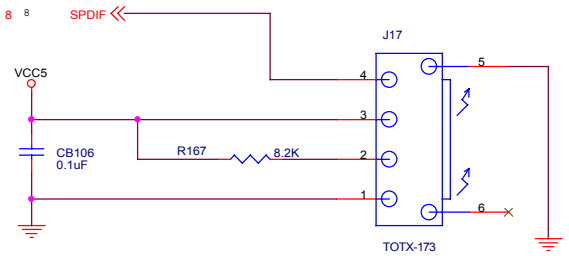
of
34



Silicon Integrated System Corp.		
Title	AC'97 CODEC(AD1881)	
Size B	Document Number SiS 55X	Rev 0.9
Date: 星期三, 七月 31, 2002	Sheet 27 of 34	

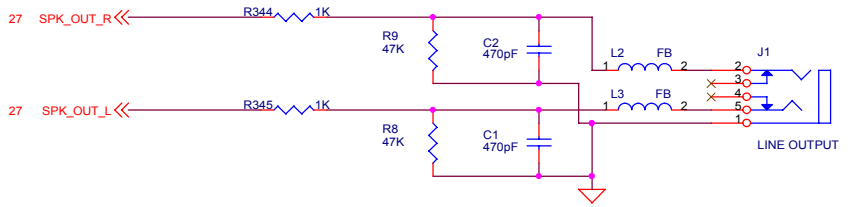
Digital Output (SPDIF)

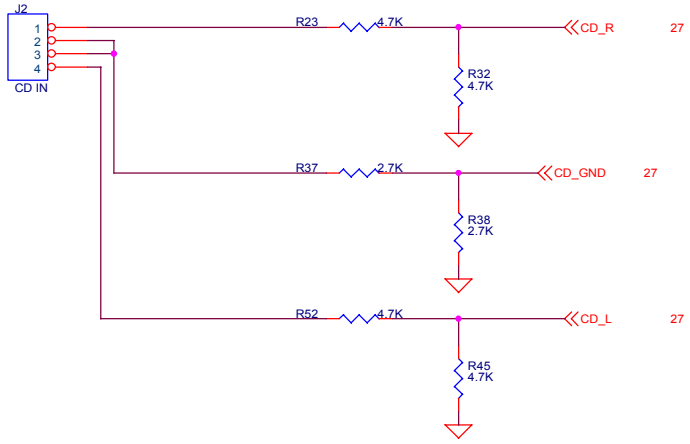


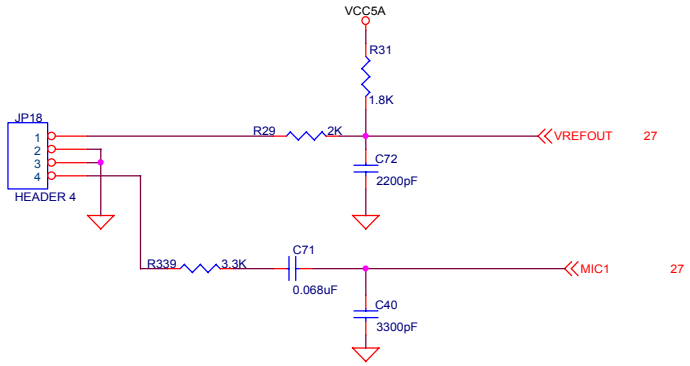
Toshiba Fiber Optic Transmitting Module
Pin connection

1. GND
2. Current limiting resistor to LED
3. VCC
4. SPDIF INPUT
5. SOLDER TO PC BOARD
6. SOLDER TO PC BOARD

AUDIO OUTPUT

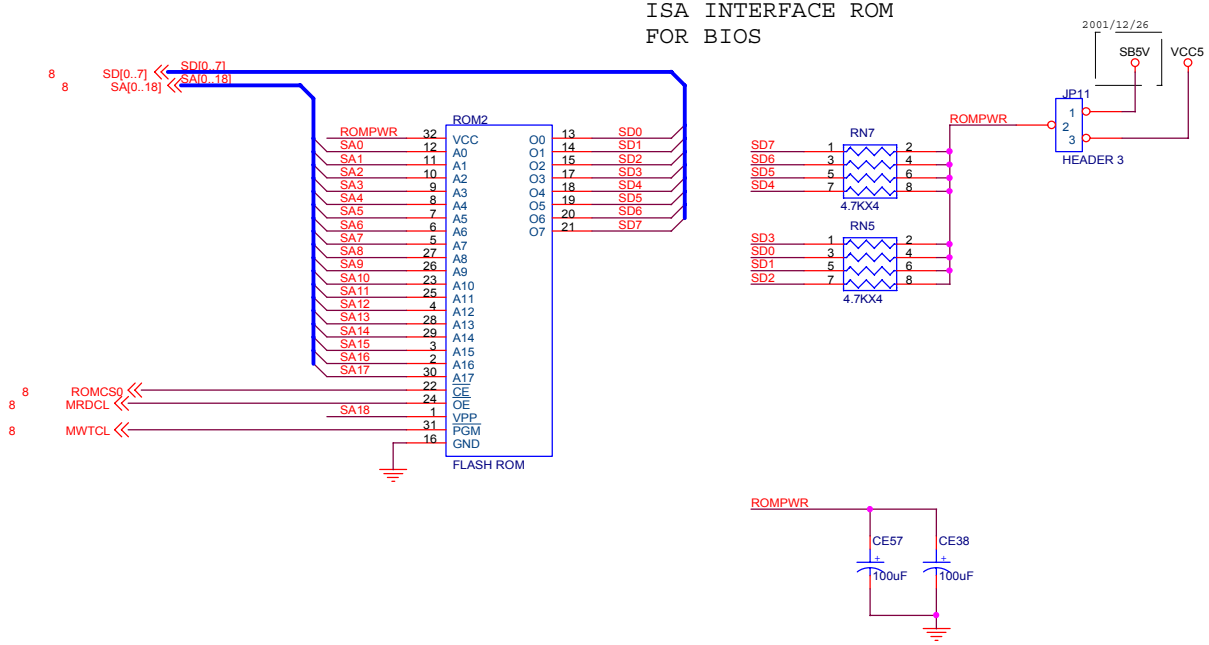






SILICON INTEGRATED SYST EM CORP		
Title: AUDIO OUTPUT		
Size: B	Document Number: SIS 55X	Rev: 0.9
Date: 星期三, 七月 31, 2002	Sheet 28 of 34	

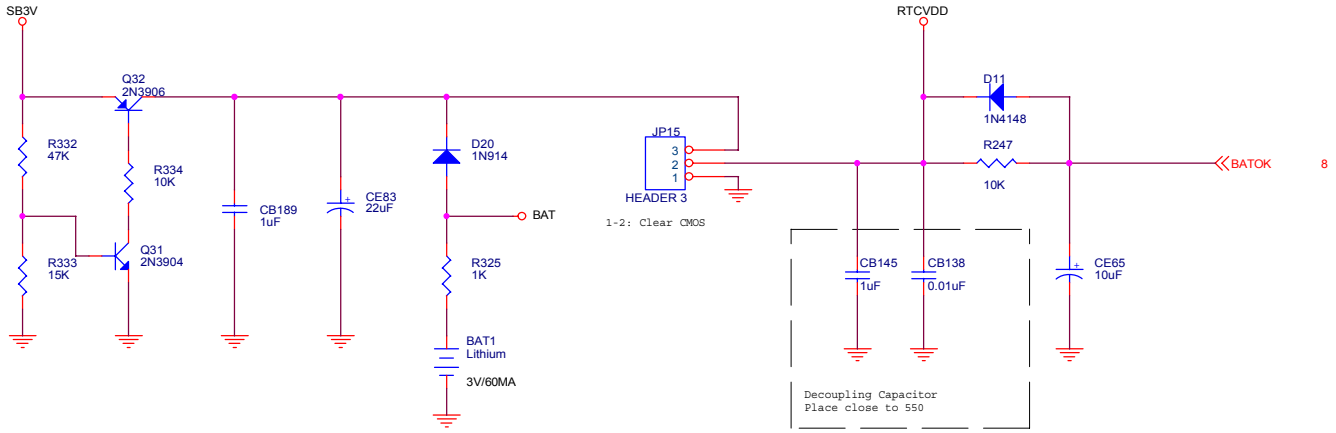
ISA INTERFACE ROM FOR BIOS

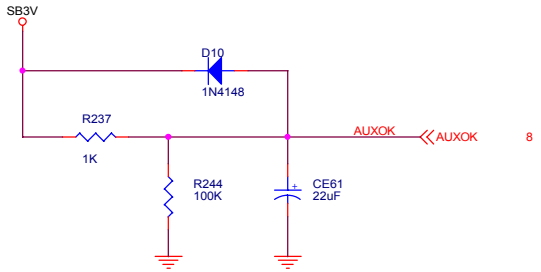


SILICON INTEGRATED SYSTEMS CORP.		
Title: ROM & LPC_CONN		
Size: B	Document Number: SiS 55X	Rev: 0.9
Date: 星期三, 七月 31, 2002	Sheet 29 of 34	

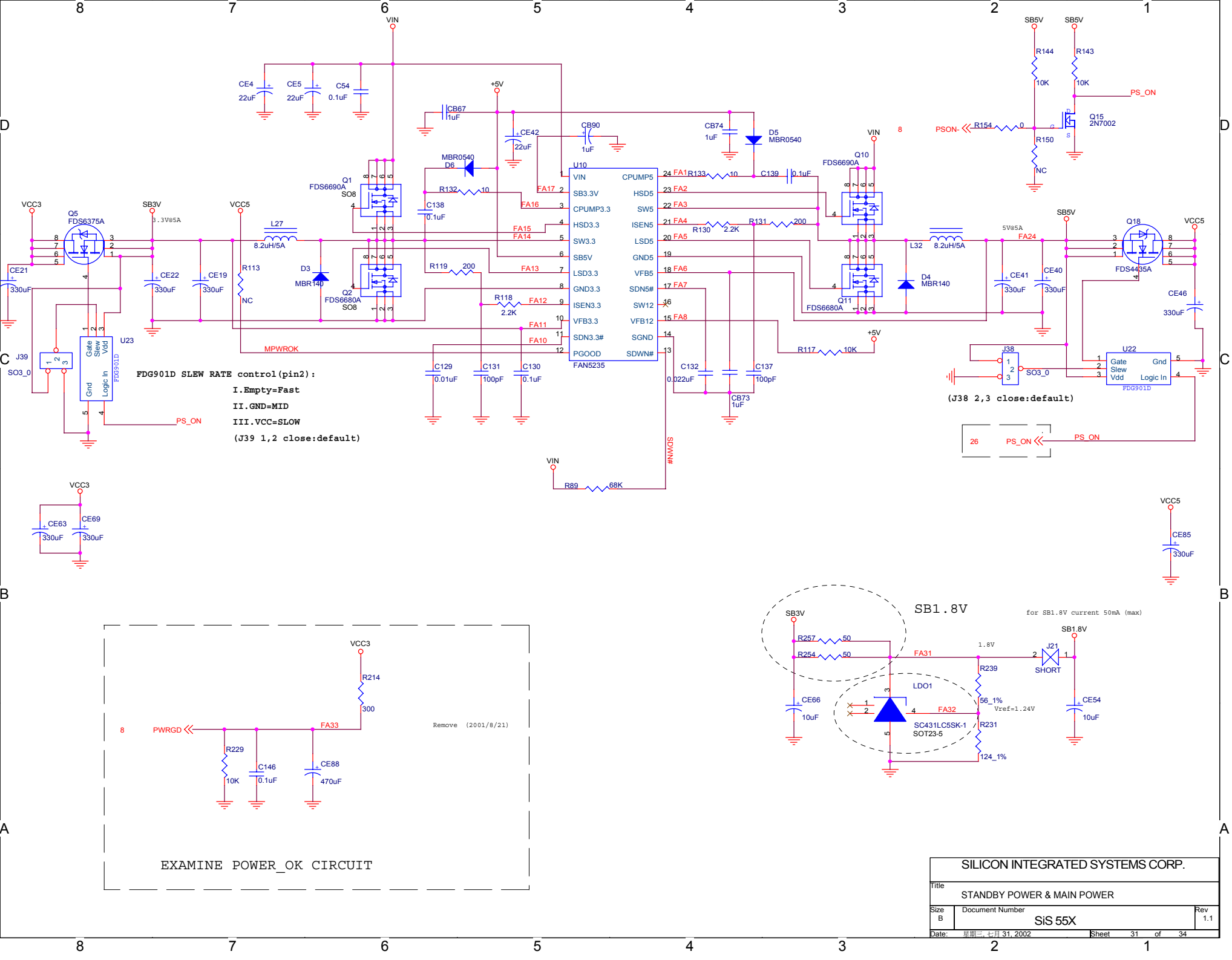
RTC

NOTE!
1.The RTCVDD is 3.3V
2.Decoupling capacitor must be close to 55X RTCVDD pin.
3.RTC circuit must strictly follow SiS's recommended design
  SiS is not responsible for RTC problems from foreign designs.

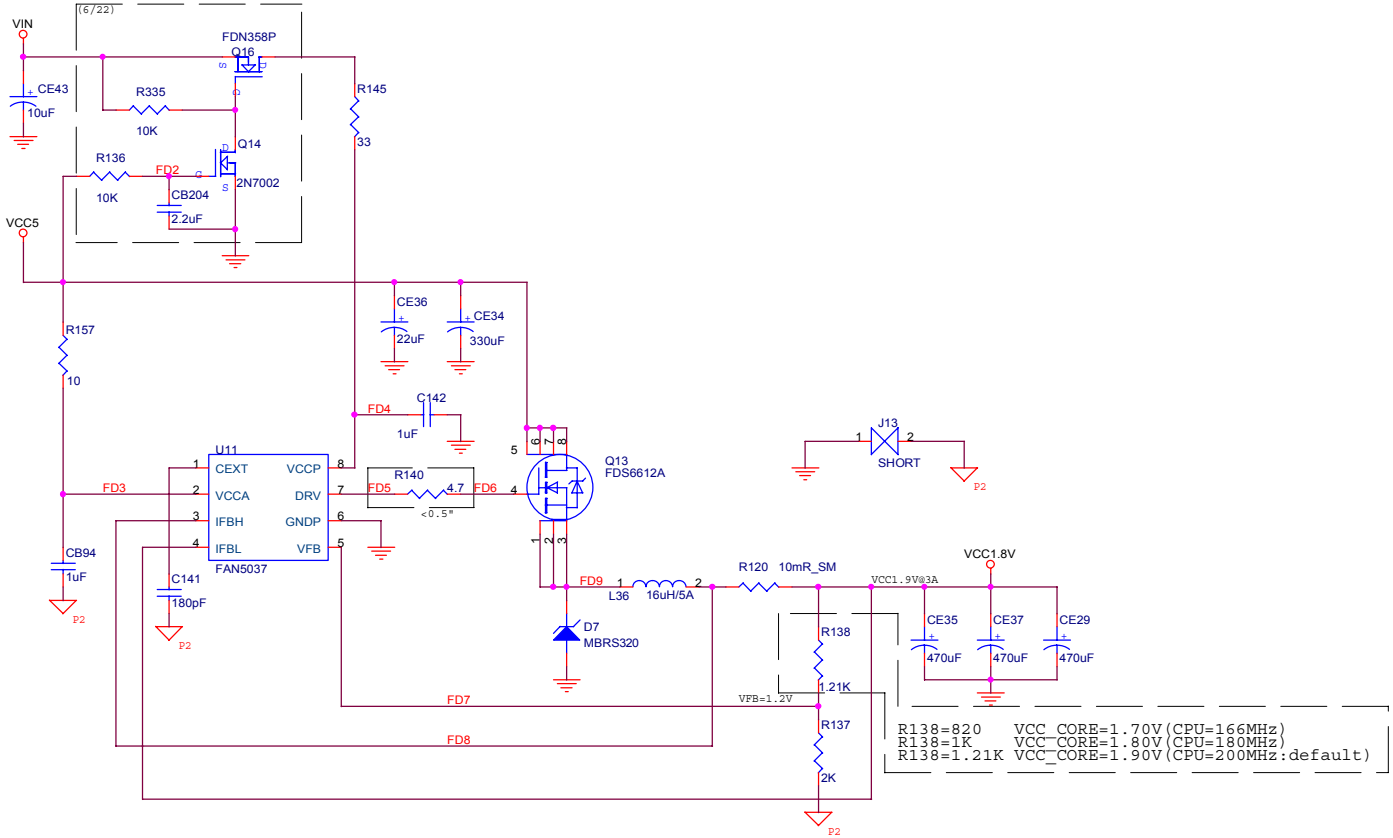




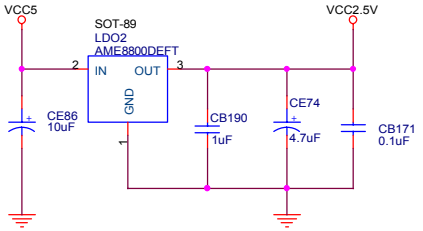
SILICON INTEGRATED SYSTEMS CORP.		
Title: RTC		
Size: B	Document Number: SiS 55X	Rev: 0.9
Date: 星期三, 七月 31, 2002	Sheet 30 of 34	

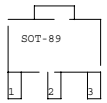


SILICON INTEGRATED SYSTEMS CORP.	
Title	STANDBY POWER & MAIN POWER
Size B	Document Number SiS 55X
Rev	1.1
Date:	星期三, 七月 31, 2002
Sheet	31 of 34



VCC2.5V





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Title: VCC1.8V & VCC2.5V		
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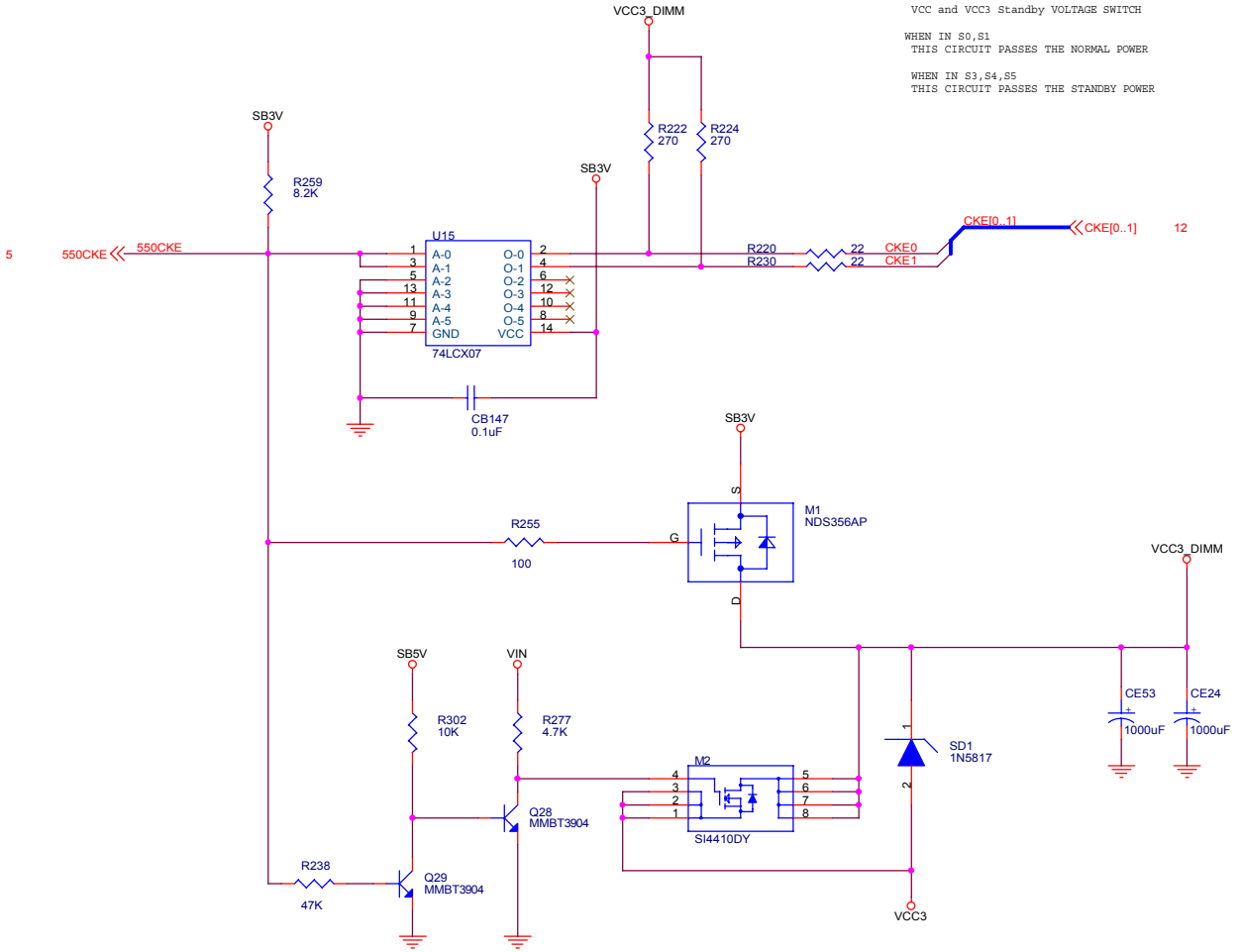

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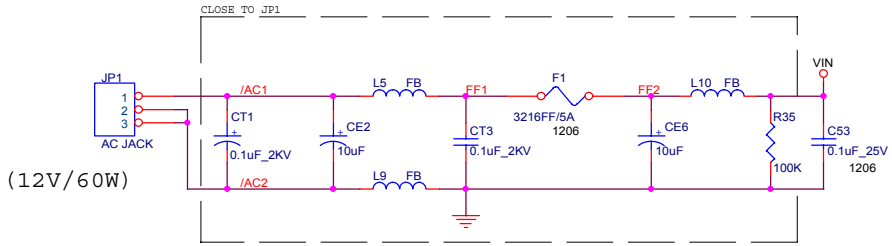

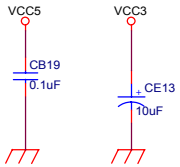

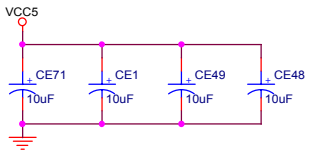

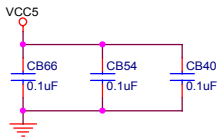

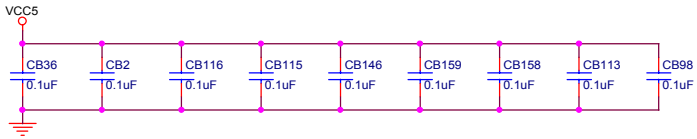

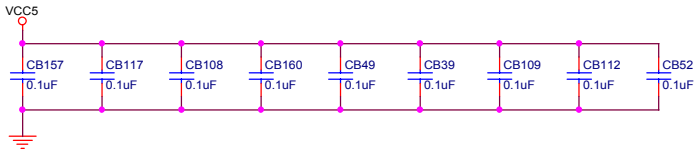

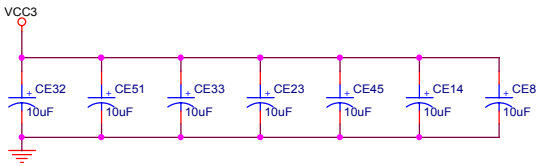

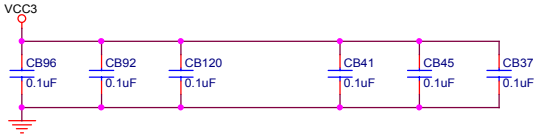

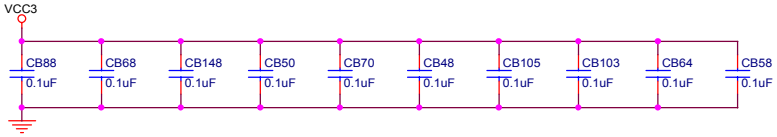

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